

# PLM-1 Powerline Modem

## User Manual





**Document version**

Version 4.0

April 2012

**Notice**

No part of this document may be copied, disclosed or conveyed to any party in any manner whatsoever without prior permission from Ariane Controls.

### About this manual

This manual is intended to give comprehensive background and design guidelines that will allow PLM-1 users to easily integrate the IC into their application.

The document begins with typical data sheet information, including package properties, pinout, electrical characteristics and operating conditions. It is followed by an overview of the PLM-1 technology, which highlights its main features and introduces the architecture of a typical PLM-1-based transceiver.

The next chapter describes the internal operation of the PLM-1 modem. The topic is organized in two parts. An introductory section, which addresses typical user, provides basic information and introduces key concepts about the PLM-1 operation. The second part includes detailed description of the internal structure and is intended as a reference for advanced users wishing to tune the chip configuration.

Sections 5 to 8 are directed toward firmware developers, describing chip configuration, control codes, packet format, interfacing with a CPU and data transmission/reception procedures.

Then, the manual presents the hardware configuration and operation of a typical communication node. Schematics and design guidelines of analog front-end circuits and power supply are provided in sections 9 and 10. Chapter 11 describes a simple testing procedure for verifying the performance of PLM-1-based transceivers.

Finally, an addendum includes extra information intended to help designers in easily integrating the PLM-1 in their project. Appendix A lists several examples of PLM-1 configurations, recommended for different communication frequencies and data rates. Appendix B provides reference schematics and lists of components for analog front-end circuits adapted to various applications.

Customers facing project requirements not covered in this document are encouraged to contact the Ariane Controls engineering team at [support@arianecontrols.com](mailto:support@arianecontrols.com).

## Table of Contents

<b>1</b>	<b>PACKAGE DESCRIPTION</b>	<b>8</b>
1.1	PINOUT	8
1.2	PIN DESCRIPTIONS	9
<b>2</b>	<b>SPECIFICATIONS</b>	<b>11</b>
2.1	RECOMMENDED OPERATING CONDITIONS	11
2.2	ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING CONDITIONS)	11
2.3	MECHANICAL PACKAGE DATA	13
<b>3</b>	<b>OVERVIEW</b>	<b>14</b>
3.1	PLM-1-BASED TRANSCEIVERS	14
3.2	COMPLIANCE WITH REGULATIONS	15
3.3	TERMINOLOGY	15
<b>4</b>	<b>FUNCTIONAL DESCRIPTION</b>	<b>16</b>
4.1	MODULATION TECHNIQUE	16
4.2	INTERNAL OPERATION OVERVIEW	17
4.2.1	CLOCKS	17
4.2.2	COMMUNICATION PORT	17
4.2.3	TRANSMITTER OPERATION	18
4.2.4	RECEIVER OPERATION	18
4.3	ADVANCED INTERNAL OPERATION	19
4.3.1	CLOCKS	19
4.3.2	TRANSMITTER	20
4.3.3	RECEIVER OPERATION	25
4.3.4	HOST INTERFACE	32
<b>5</b>	<b>CONFIGURATION PARAMETERS</b>	<b>33</b>
5.1	COMMUNICATION PARAMETERS	33
5.1.1	BASIC COMMUNICATION PARAMETERS	34
5.1.2	ADVANCED COMMUNICATION PARAMETERS	34
5.2	MAC PARAMETERS	35
5.3	HARDWARE PARAMETERS	36

<b>5.4</b>	<b>INITIALIZATION SEQUENCE</b>	<b>39</b>
5.4.1	CRC	39
<b>6</b>	<b>CONTROL CODES</b>	<b>40</b>
<b>6.1</b>	<b>INPUT CONTROL CODES</b>	<b>40</b>
6.1.1	END OF FIELD – 10H (EOF)	40
6.1.2	END OF PACKET – 11H (EOP)	40
6.1.3	DISABLE RECEIVER – 12H (DISR)	40
6.1.4	START TIMER - 14H (STRT)	41
6.1.5	STOP TIMER - 15H (STOT)	41
6.1.6	RESET – 16H (RESET)	41
6.1.7	NO OPERATION – 1FH (NOP)	41
<b>6.2</b>	<b>OUTPUT CONTROL CODES</b>	<b>41</b>
6.2.1	END OF FIELD – 10H (EOF)	41
6.2.2	END OF PACKET – 11H (EOP)	41
6.2.3	ERROR RECEIVED – 12H (ERR)	41
6.2.4	RECEIVER OVER-RUN – 13H (ROVR)	41
6.2.5	COLLISION – 14H (COLL)	42
6.2.6	TRANSMITTER UNDER-RUN – 17H (TUNR)	42
6.2.7	TRANSMITTER REGISTER EMPTY – 18H (TXRE)	42
6.2.8	TRANSMITTER OVER-RUN – 19H (TOVR)	43
6.2.9	TIMER ELAPSED - 1AH (TEL)	43
6.2.10	TIMER OVERRUN - 1AH (TOVR)	43
6.2.11	NO OPERATION – 1FH (NOP)	43
<b>7</b>	<b>PACKET FORMAT</b>	<b>44</b>
<b>7.1</b>	<b>FIRST NIBBLE</b>	<b>44</b>
<b>7.2</b>	<b>CHANNEL</b>	<b>44</b>
<b>7.3</b>	<b>ADDRESSING</b>	<b>44</b>
<b>8</b>	<b>INTERFACING WITH A CPU</b>	<b>46</b>
<b>8.1</b>	<b>HOST INTERFACE</b>	<b>46</b>
8.1.1	POLLING	46
8.1.2	PARALLEL PORT	47
8.1.3	SERIAL PERIPHERAL INTERFACE (SPI)	49
<b>8.2</b>	<b>CONFIGURATION PROCEDURE</b>	<b>51</b>
<b>8.3</b>	<b>TRANSMITTING AND RECEIVING</b>	<b>52</b>
8.3.1	CONFIGURING	52
8.3.2	IDLE	52
8.3.3	NEGOTIATING	52
8.3.4	TRANSMITTING	53
8.3.5	RECEIVING	53

---

<b>9</b>	<b><u>ANALOG FRONT-END</u></b>	<b>54</b>
<b>9.1</b>	<b>AFE OPERATION</b>	<b>54</b>
9.1.1	RX CIRCUIT	54
9.1.2	TX CIRCUIT	54
9.1.3	COUPLING CIRCUIT	55
<b>9.2</b>	<b>FILTER DESIGN</b>	<b>55</b>
9.2.1	FILTER CHARACTERISTICS	55
9.2.2	FILTER EXAMPLES	57
<b>9.3</b>	<b>LINE DRIVER DESIGN</b>	<b>61</b>
9.3.1	LINE DRIVER CHARACTERISTICS	61
9.3.2	LINE DRIVER OPTIONS	62
<b>9.4</b>	<b>COUPLING CIRCUIT DESIGN</b>	<b>65</b>
9.4.1	COUPLING CIRCUIT CHARACTERISTICS	65
9.4.2	COUPLING METHODS	65
<b>9.5</b>	<b>AFE REFERENCE DESIGNS</b>	<b>68</b>
<b>10</b>	<b><u>POWER SUPPLIES FOR PLM-1 TRANSCEIVERS</u></b>	<b>69</b>
<b>10.1</b>	<b>POWER SUPPLY CHARACTERISTICS</b>	<b>69</b>
10.1.1	OUTPUT POWER	69
10.1.2	INPUT IMPEDANCE	69
10.1.3	NOISE	70
<b>10.2</b>	<b>POWER SUPPLY OPTIONS</b>	<b>70</b>
10.2.1	LINEAR POWER SUPPLY	70
10.2.2	SWITCHING-MODE POWER SUPPLY	71
10.2.3	CAPACITIVE POWER SUPPLY	71
10.2.4	ENERGY STORAGE POWER SUPPLY	72
<b>11</b>	<b><u>TRANSCEIVER PERFORMANCE VERIFICATION</u></b>	<b>73</b>
<b>11.1</b>	<b>TEST SETUP</b>	<b>73</b>
<b>11.2</b>	<b>TRANSCEIVER INFLUENCE VERIFICATION</b>	<b>74</b>
<b>11.3</b>	<b>TRANSMIT PERFORMANCE VERIFICATION</b>	<b>74</b>
<b>11.4</b>	<b>RECEIVE PERFORMANCE VERIFICATION</b>	<b>74</b>
<b>11.5</b>	<b>SUMMARY OF RESULTS</b>	<b>75</b>
<b>12</b>	<b><u>APPENDICES</u></b>	<b>76</b>
<b>APPENDIX A</b>	<b>RECOMMENDED PLM-1 CONFIGURATIONS</b>	<b>76</b>
<b>APPENDIX B</b>	<b>ANALOG FRONT-END REFERENCE SCHEMATICS</b>	<b>77</b>

# 1 Package Description

## 1.1 Pinout

Figure 1-1 shows the pinout diagram of the PLM-1 modem.

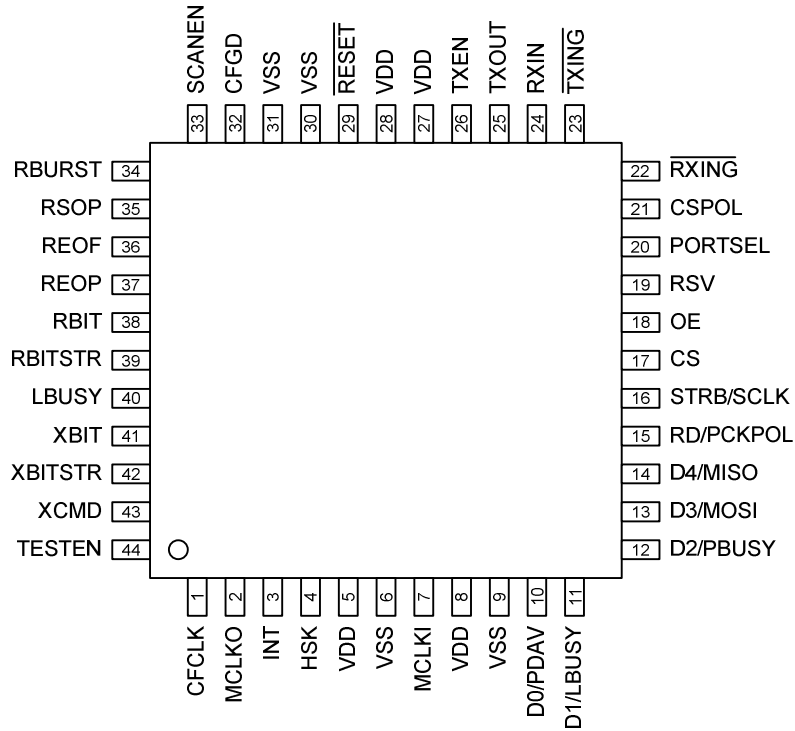


Figure 1-1 PLM-1 package pinout

## 1.2 Pin Descriptions

Name	Pin	Type	Description
CFCLK	1	Output	Reference frequency clock. Outputs a square wave of frequency $f_{ref}$ when the chip is configured.
MCLKO	2	Output	Master clock output. Its frequency is $f_{osc}$ . This pin outputs an image of MCLKI.
INT <sup>2</sup>	3	Output / High-Z	Interrupt. This pin can be configured to be active-low or active-high.
HSK <sup>2</sup>	4	Output / High-Z	Handshake. During a host parallel READ operation, HSK is set High to indicate that data is available on pins D0-D4. During a host WRITE operation, HSK is set High to indicate that the PLM-1 has sampled data on pins D[4:0]. HSK is in a high impedance state when CS is deactivated.
VDD	5, 8, 27, 28	Supply	3.3V power supply terminals.
VSS	6, 9, 30, 31	Supply	Ground terminals.
MCLKI	7	Input	Master clock input ( $f_{osc}$ ). This pin must be driven by an external electronic oscillator or microcontroller. Do not connect a crystal to this pin.
D0/PDAV <sup>1,2</sup>	10	Input / Output	Parallel port: Data I/O 0 / Data Available. During a READ operation, while STRB/SCLK is Low, this pin also indicates that data is available on the parallel port. SPI port: Data Available. PDAV is active high.
D1/LBUSY <sup>1,2</sup>	11	Input / Output	Parallel port: Data I/O 1 / Line busy. During a READ operation, while STRB/SCLK is Low, this pin also indicates that the line is busy. SPI port: Line Busy. LBUSY is active high.
D2/PBUSY <sup>1,2</sup>	12	Input / Output	Parallel port: Data I/O 2 / Port Busy. During a READ operation, while STRB/SCLK is Low, this pin also indicates that the parallel port is busy. SPI port: Port Busy. PBUSY is active high.
D3/MOSI <sup>1,2</sup>	13	Input / Output	Parallel port: Data I/O 3. SPI port: MOSI - Master Output Slave Input (serial data input of PLM-1).
D4/MISO <sup>1,2</sup>	14	Input / Output / High-Z	Parallel port: Data I/O 4. SPI port: MISO - Master Input Slave Output (serial data output of PLM-1). MISO provides a high impedance state when CS is deactivated.
RD/PCKPOL <sup>1,2</sup>	15	Input	Parallel port: Read/Write control signal. When driven High, RD indicates a read access from the PLM-1. When driven Low, RD indicates a write access to the PLM-1. SPI port: Clock Polarity. This pin configures how the PLM-1 samples and setup the data on the MOSI and MISO lines respectively, as well as specifying the default level of the clock when the SPI port is idle.
STRB/SCLK <sup>1,2</sup>	16	Input	Parallel port: READ or WRITE strobe signal. SPI port: Serial Clock. The maximum frequency of SCLK is $f_{osc}/4$ .
CS <sup>1,2</sup>	17	Input	Chip-Select for parallel and SPI ports. This pin can be configured to be active low or active high.

## AC-PLM-1

Name	Pin	Type	Description
OE <sup>2</sup>	18	Output	Output Enable. This pin is asserted High when using the parallel port, the CS pin is active and the RD line is High. In normal operation, this signal is not needed and it can be left unconnected. This signal can be used to control external tristate buffers for the data lines D0-D4, e.g. when using the parallel port of a PC to directly interface to the PLM-1.
RSV <sup>2</sup>	19	Output	Reserved (leave unconnected, do not connect to power or ground)
PORTSEL <sup>1,2</sup>	20	Input	Communication port type selection. High to select the parallel port. Low to select the SPI port.
CSPOL <sup>1,2</sup>	21	Input	Chip-Select Polarity. When this pin is High, CS is active high. When it is Low, CS is active low.
$\overline{\text{RXING}}$	22	Output	Receiving. This pin is asserted Low when the PLM-1 is receiving a packet. This pin can drive a LED directly.
$\overline{\text{TXING}}$	23	Output	Transmitting. This pin is asserted Low when the PLM-1 is transmitting a packet. This pin can drive a LED directly.
RXIN <sup>2</sup>	24	Input	Receiver Input.
TXOUT <sup>2</sup>	25	Output	Transmitter Output.
TXEN <sup>2</sup>	26	Output	Transmitter Output Enable. This pin is active when the PLM-1 is transmitting. It can be used to put the external power amplifier into a low-power mode when the PLM-1 is not transmitting. Its polarity can be configured through the TXENPOL configuration parameter.
$\overline{\text{RESET}}$	29	Input	Logic Reset input. Asserting this terminal Low resets the internal logic.
CFGD	32	Output	Configuration Done. The PLM-1 asserts this pin High when it has successfully received and verified the CRC of its configuration data. This pin can drive a LED directly.
SCANEN <sup>3</sup>	33	Input	Test Control input (for Ariane Controls internal use only). In normal operation, this pin must be tied to ground.
RBURST <sup>4</sup>	34	Output	Positive pulse when a preamble burst is detected.
RSOP <sup>4</sup>	35	Output	Goes high when a Start of Packet symbol is received.
REOF <sup>4</sup>	36	Output	Goes high when a End of Field symbol is received.
REOP <sup>4</sup>	37	Output	Goes high when a End of Packet symbol is received.
RBIT <sup>4</sup>	38	Output	Received bit.
RBITSTR <sup>4</sup>	39	Output	Received bit strobe. Pulse indicating moments when RBIT is sampled.
LBUSY <sup>4</sup>	40	Output	High when the communication channel is busy.
XBIT <sup>4</sup>	41	Output	Bit transmitted. Only valid when TXEN is active.
XBITSTR <sup>4</sup>	42	Output	Indicates the moment when the transmitted bit changes.
XCMD <sup>4</sup>	43	Output	High when the modem is transmitting and the preamble is over.
TESTEN <sup>1</sup>	44	Input	Enables pins 34 to 43. Active high.

### Notes:

1. Pin with internal 50k $\Omega$  pull-up resistor.
2. 5V tolerant pin.
3. Pin with internal 50k $\Omega$  pull-down resistor.
4. Pin only active if TESTEN is high.

## 2 Specifications

### 2.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply Voltage	3.0	3.3	3.6	V
$f_{osc}$	Clock Frequency	4.0		20 Note 1	MHz
$f_c$	Communication Center Frequency	50		500	kHz
$T_a$	Ambient Temperature	-40	25	85	°C

### 2.2 Electrical Characteristics (over recommended operating conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low-Level Voltage (3V TTL or 5V TTL Tolerant)			0.8	V
$V_{IH}$	Input High-Level Voltage (3V TTL or 5V TTL Tolerant)	2.0			V
$V_{OL}$	Output Low-Level Voltage			0.4	V
$V_{OH}$	Output High-Level Voltage	2.4			V
$I_{DDi}$	Supply Current in Idle Mode		7.3	8.5	mA
$I_{DDo}$	Supply Current in Receive or Transmit Mode		16	16.5	mA
$I_o$	Output current			3	mA
$f_b$	PHY Data Rate			30.8 Note 2	kbps

**Notes:**

1. The maximum clock frequency is related to the communication frequency. See Figure 2-1.
2. The maximum data rate depends on the communication frequency. See Figure 2-2 .

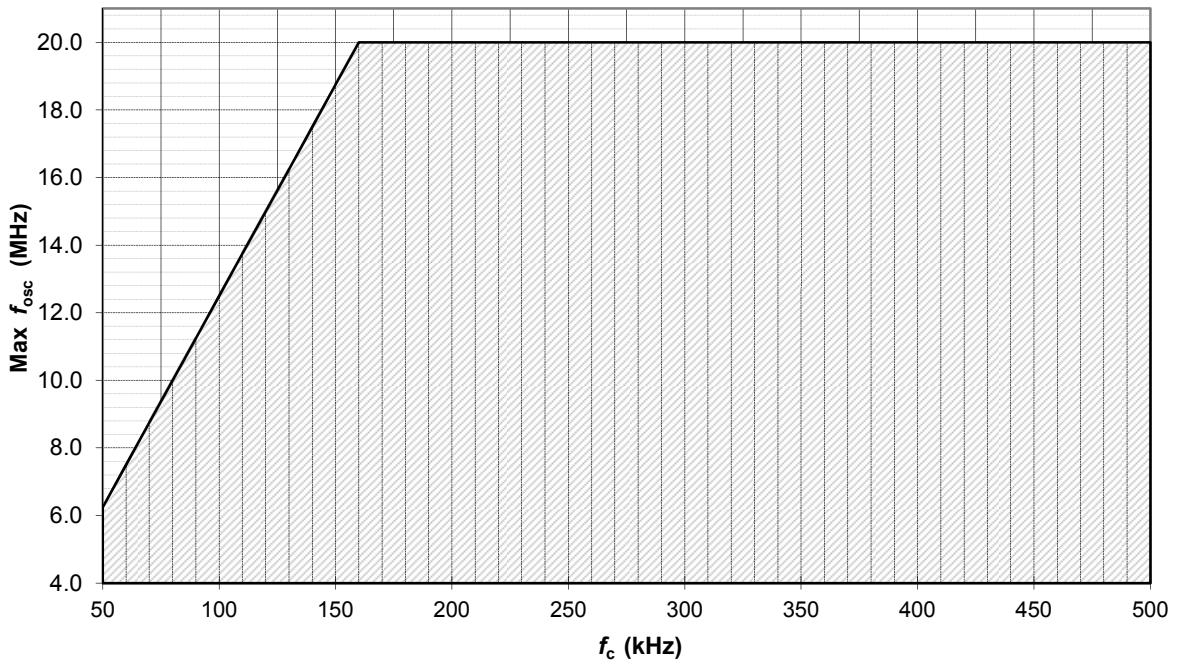


Figure 2-1 Maximum clock frequency versus communication center frequency

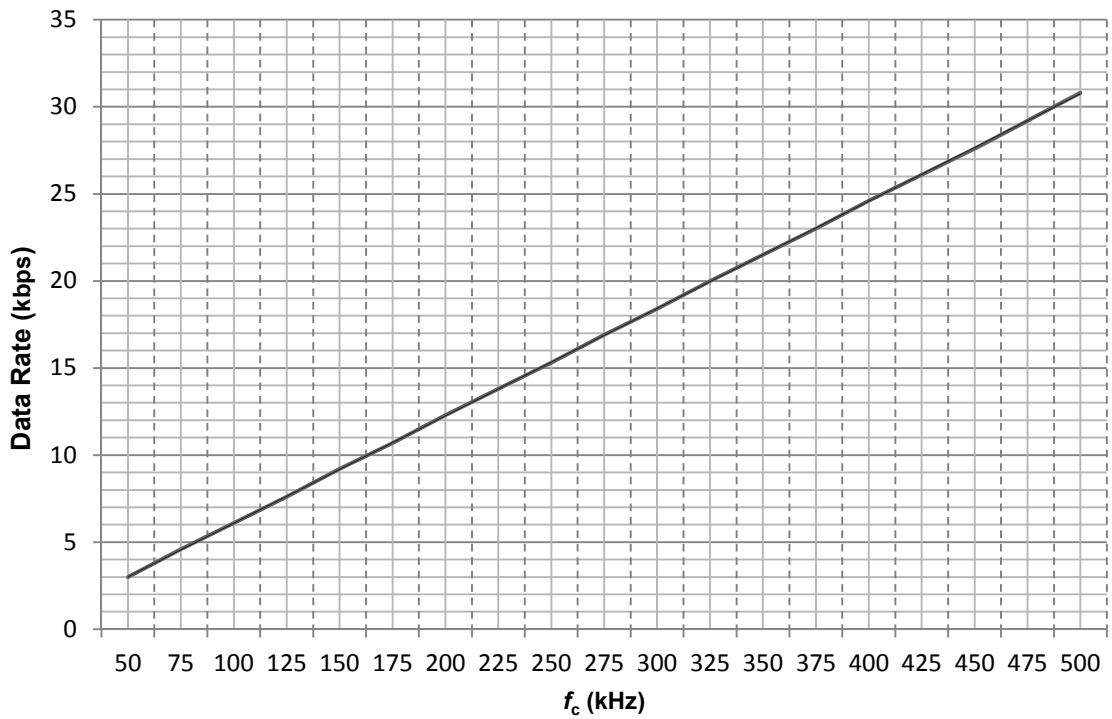


Figure 2-2 Maximum PHY data rate versus communication frequency

## 2.3 Mechanical Package Data

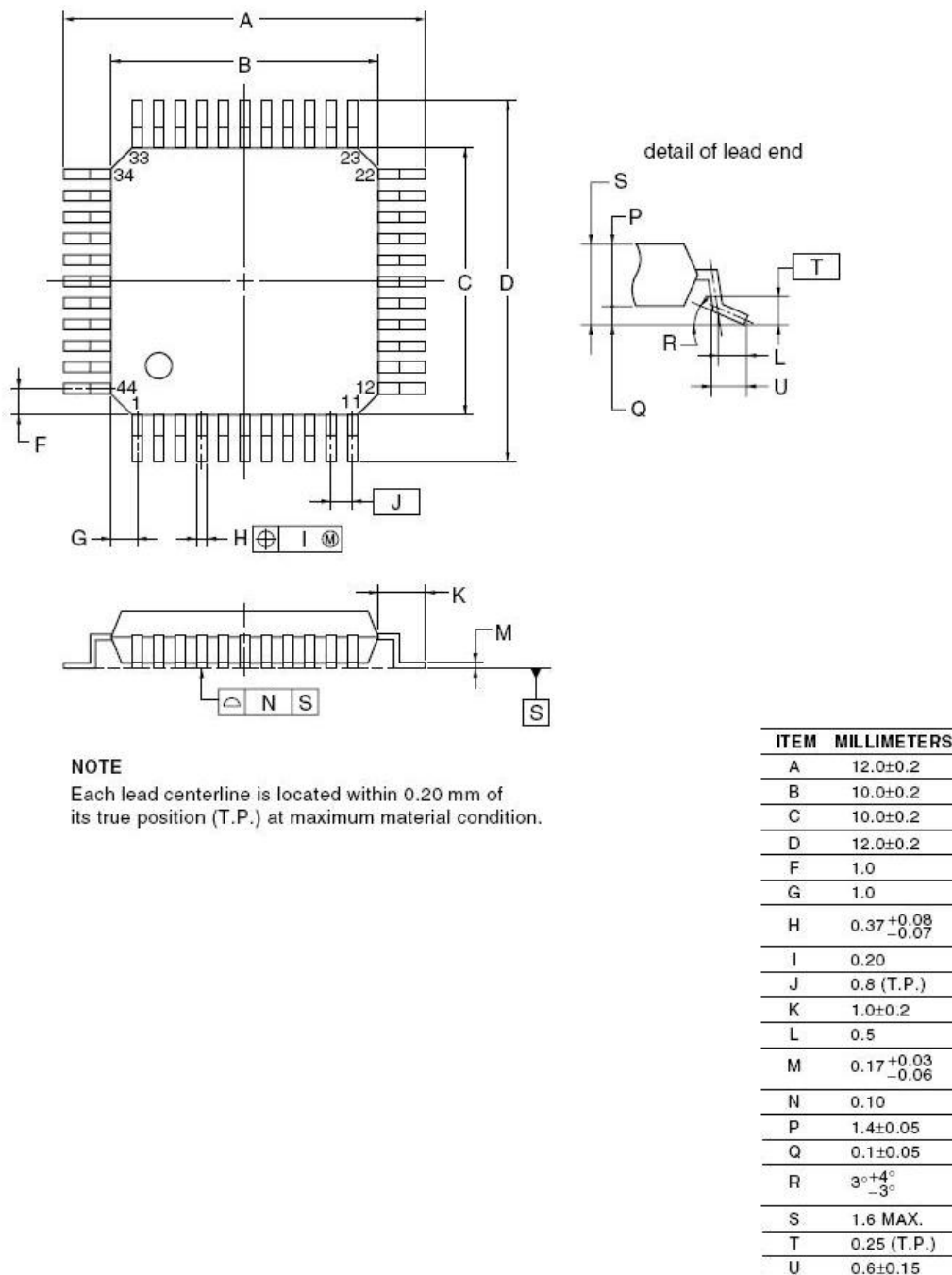


Figure 2-3 PLM-1 LQFP-44 package

### 3 Overview

The PLM-1 is a fully digital data transceiver for powerline communications using Frequency-Shift Keying (FSK). This ASIC is a very efficient solution for cost sensitive, medium data rate applications.

The PLM-1 is designed to be controlled from an external Central Processing Unit, most commonly a microcontroller (MCU), which is referred to as the *host* throughout this text.

Implementing the PHY and MAC layers of the OSI model, the PLM-1 provides a way to efficiently modulate and demodulate data packets. It features collision detection, as well as automatic forward error correction and CRC-16 data integrity verification. Higher-level functions such as addressing and networking are handled by the host if needed.

The PLM-1 patented technology offers the advantage of being highly configurable. It allows communicating at any frequency between 50kHz and 500kHz with data rates up to 30kbps (see Figure 2-2).

#### 3.1 PLM-1-based transceivers

The PLM-1 modem can be used to transport data over any AC, DC or unpowered line. The external circuitry can be adapted to meet the characteristics and requirements of various applications, e.g. line conditions, applicable regulations, node size and cost.

Figure 3-1 presents the block diagram of a typical PLM-1-based powerline transceiver. The main external components required to complete the PLM-1 modem functionality are:

- Host microcontroller (MCU): implements the upper layers of the communication protocol and application specific functions.
- Oscillator (Osc): provides the operating clock signal.
- Analog Front End: performs signal conditioning and coupling with the communication lines.
- Power supply: provides suitable DC power to all components.

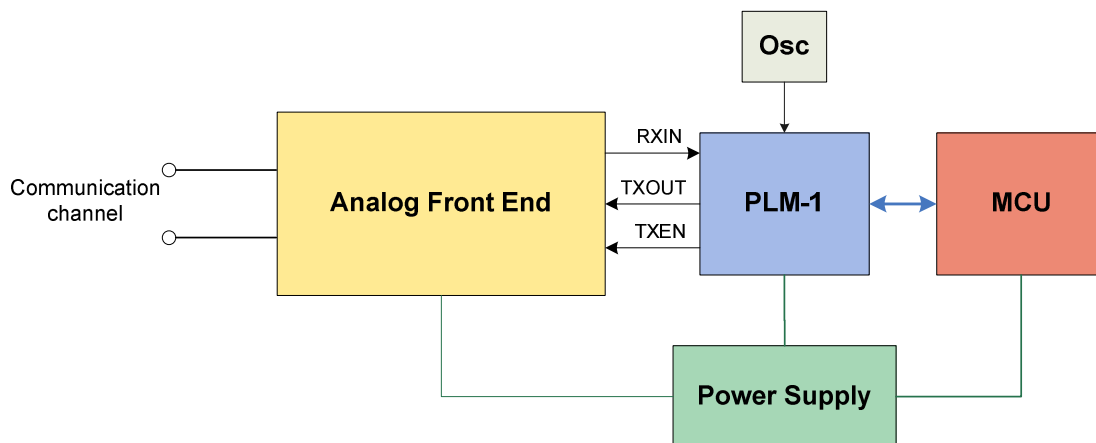


Figure 3-1 Block diagram of PLM-1-based powerline transceiver

#### Features

- Robust narrowband FSK modulation
- Transmission data rate up to 30kbps
- Programmable communication frequency from 50kHz to 500kHz
- Complete Media Access Control (MAC) logic
- CSMA/CD type collision detection and resolution
- Packet priority management
- Error detection (CRC-16)
- High-efficiency Forward Error Correction
- Parallel and SPI interfaces
- Protocol neutral

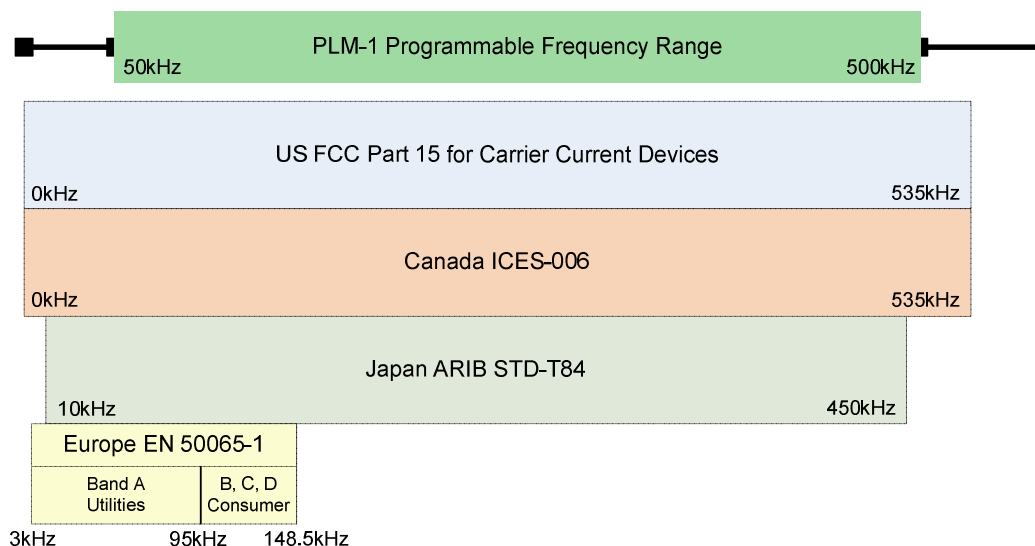


Figure 3-2 PLM-1 programmable frequency range

## 3.2 Compliance with regulations

Powerline communications are governed by national and international standards that set limits and rules to prevent interference and to facilitate the coexistence of different devices and technologies. However, there are differences between the regional regulations, mainly concerning the frequency band allocation, the output power levels, and the electromagnetic emissions.

PLM-1-based transceivers can be designed to comply with the main international regulatory standards (e.g., US FCC part 15, Industry Canada NMB-006, Japan's ARIB, Europe's CENELEC EN50065-1), allowing them to be used in worldwide applications (Figure 3-2).

## 3.3 Terminology

The PLM-1 modem can be used to transport data over many mediums, such as AC or DC power lines, twisted pair or un-powered lines. Hence, in this document the terms communication *medium* or *channel* are used, to be more general.

The PLM-1 is designed to be controlled from an external Central Processing Unit, most commonly a microcontroller (MCU), which is referred to as the *host* throughout this text.

To avoid confusion between the communication host - PLM-1 and powerline communication, the terms transmission and reception refer exclusively to communication over the medium. The term *write* describes data transfer from the host to the PLM-1 whereas *read* describes data transfer from the PLM-1 to the host, unless explicitly specified.

PLM-1 pins are written with bold-faced capital letters. Example: **CFCLK**.

Configuration parameters and control codes use capital letters. Example: XDIV.

Variables that appear in mathematical equations use italics. Example:  $f_{ref}$ .

## 4 Functional Description

### 4.1 Modulation Technique

The narrowband FSK modulation technique used by the PLM-1 encodes data in a binary signal whose frequency is shifted between two discrete values:  $f_0$  for logic 0 and  $f_1$  for logic 1. The average value of the two frequencies is defined as the center frequency  $f_c$ .

By mixing an internal configurable frequency  $f_{ref}$  with lower frequencies  $\Delta f_0$  or  $\Delta f_1$ , the PLM-1 generates two frequency pairs:  $(f_{L1}, f_{L0})$  and  $(f_{H1}, f_{H0})$ .

$$f_{L0} = f_{ref} - \Delta f_0 \quad (1)$$

$$f_{L1} = f_{ref} - \Delta f_1 \quad (2)$$

$$f_{H0} = f_{ref} + \Delta f_0 \quad (3)$$

$$f_{H1} = f_{ref} + \Delta f_1 \quad (4)$$

As all these frequency components are output on the **TXOUT** pin of the PLM-1. An external analog filter with band-pass characteristic is used to select one frequency pair as the  $f_0$  and  $f_1$  communication frequencies. Figure 4-1 presents the frequencies generated by the PLM-1 and a filter selecting  $f_{L0}$  and  $f_{L1}$  as communication frequencies  $f_0$  and  $f_1$ .

Alternatively, the higher frequencies  $(f_{H1}, f_{H0})$  can also be used as communication frequencies. In this case, the external filter would have to be centered on the average of  $f_{H0}$  and  $f_{H1}$ .

The difference between  $f_0$  and  $f_1$  is narrow, usually about a few kHz. This is a key feature of the PLM-1

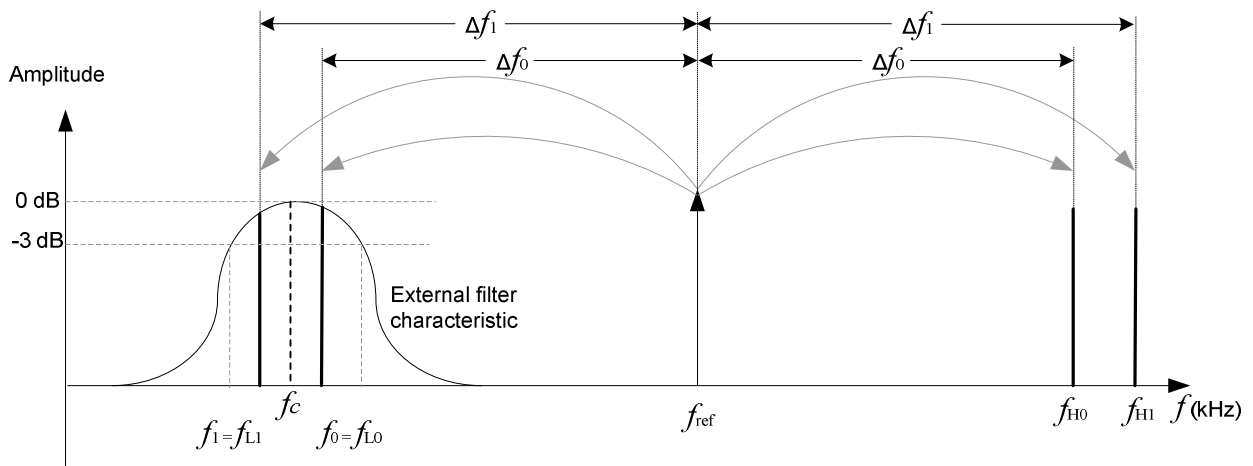


Figure 4-1 Generation and selection of communication frequencies

technology, since it provides high noise immunity on the receiver side. External band-pass filters with a minimum bandwidth to pass  $f_0$  and  $f_1$  are required in reception and transmission paths. The filter in reception rejects noise from the power lines and all signals at other frequencies. The filter in transmission converts the PLM-1 binary output in sinusoidal signal and removes the  $f_{ref}$  frequency component, the two unselected frequencies and all related harmonics.

Communication bandwidth is also directly related to the data rate. The larger the bandwidth, the faster the communication can get. Consequently, choosing the optimal bandwidth is a compromise between the noise rejection capability and data transmission rate.

## 4.2 Internal Operation Overview

The internal structure of the PLM-1 consists of four main blocks, as shown in Figure 4-2. The Host Interface is used to communicate with the host MCU. The Clock Generator is used internally to set timings for communication frequencies. The Receiver demodulates data coming from **RXIN**, decodes it and feeds it to the host interface. The Transmitter receives data from the host interface and modulates them on the output signal pin **TXOUT**. The pin **TXEN** is used to enable the external amplifier during transmission.

### 4.2.1 Clocks

The PLM-1 modem needs an external clock signal **MCLKI** that ranges from 4MHz to 20MHz to provide the operating frequency  $f_{osc}$ .

A second clock of frequency  $f_{ref}$ , **CFCLK**, is generated internally by the PLM-1 to provide the reference frequency used for modulation.

### 4.2.2 Communication Port

The host communicates with the PLM-1 using a parallel or SPI interface. Communication between the host and the PLM-1 uses 5-bit symbols called *nibbles* in this manual. Hence, the parallel mode uses a 5-bit communication bus, whereas in SPI mode, the 3 msb are ignored in each byte transferred. The PLM-1 makes a distinction between *data nibbles* and *control nibbles*.

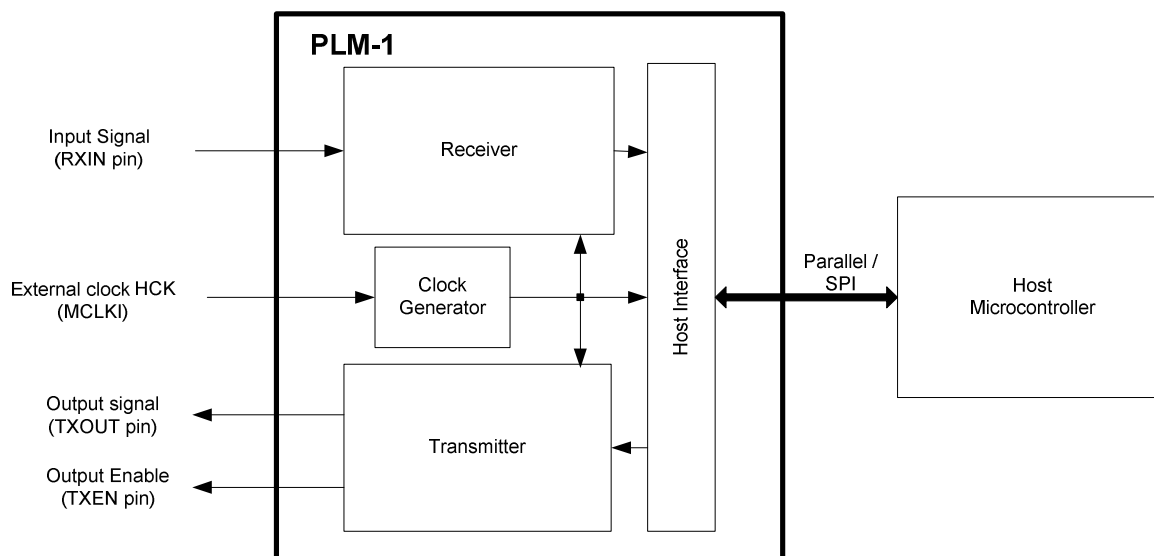


Figure 4-2 Simplified PLM-1 block diagram

Nibble type	Binary expression
Data nibble	{0, d <sub>3</sub> , d <sub>2</sub> , d <sub>1</sub> , d <sub>0</sub> }
Control nibble	{1, d <sub>3</sub> , d <sub>2</sub> , d <sub>1</sub> , d <sub>0</sub> }

**Table 4-1 Distinction between data nibbles and control nibbles**

The msb of data nibbles is 0 whereas the msb of control nibbles is 1. Table 4-1 shows this distinction.

The communication interface used is selected with the input pin **PORTSEL** (low selects SPI, high selects parallel). While it is recommended to use the SPI port for ease of implementation and portability, the use of the parallel port is suggested for hosts lacking SPI compatibility.

### 4.2.3 Transmitter Operation

The transmitter section waits for the host to load the first nibble of the packet to transmit. After a priority-queuing wait time, the PLM-1 automatically transmits a preamble in order to gain access to the communication channel. This preamble does not carry any information and is used to detect simultaneous attempts at transmission by other devices. If a communication is detected on the line, the current transmission is aborted. The host may try again when the other transmission is over. If the PLM-1 gains access to the channel, it starts transmitting host data, while automatically adding error correction codes.

The PLM-1 uses the **INT** pin to notify the host every time a new nibble is needed. The host must provide it before the current nibble transmission finishes.

A packet ends with the End of Packet control nibble. When the PLM-1 reads this code from the host, it terminates the packet by transmitting a CRC-16 value calculated internally during the entire transmission procedure.

### 4.2.4 Receiver Operation

The receiver block is always active, except while the modem is transmitting. It continuously synchronizes with incoming data. When the beginning of a packet is detected, error-corrected data starts being transferred to the host after raising the **INT** pin. Every time a nibble is decoded, the internal CRC-16 is updated and the nibble is transferred to the host, which must read it before the next one comes in. Reading an End of Packet nibble confirms the packet was successfully received. An error code can also be written to the host at any time indicating either an FEC failure or a CRC-16 mismatch.

### 4.3 Advanced Internal Operation

The PLM-1 provides many configuration parameters as well as many signals available for monitoring. This section presents an extensive look at the operation of the PLM-1 in order to explain the use of these signals and parameters. **This section may be skipped** as it is intended for advanced users. This section can be used as a reference and is not a mandatory reading in order to properly use the PLM-1. The recommended configurations and the reference designs from this manual already provide optimal communication results.

This section describes in detail the four main blocks of Figure 4-2 and expands on each of them to provide information on configuration parameters and monitoring signals of the PLM-1. Figure 4-3 presents the complete functional block diagram of the PLM-1.

#### 4.3.1 Clocks

The purpose of the Clocks block is to generate **CFCLK**, a clock of frequency  $f_{ref}$ . It is obtained by dividing frequency  $f_{osc}$  of input signal **MCLKI** by configuration register **XDIV**.

$$f_{ref} = \frac{f_{osc}}{XDIV} \tag{5}$$

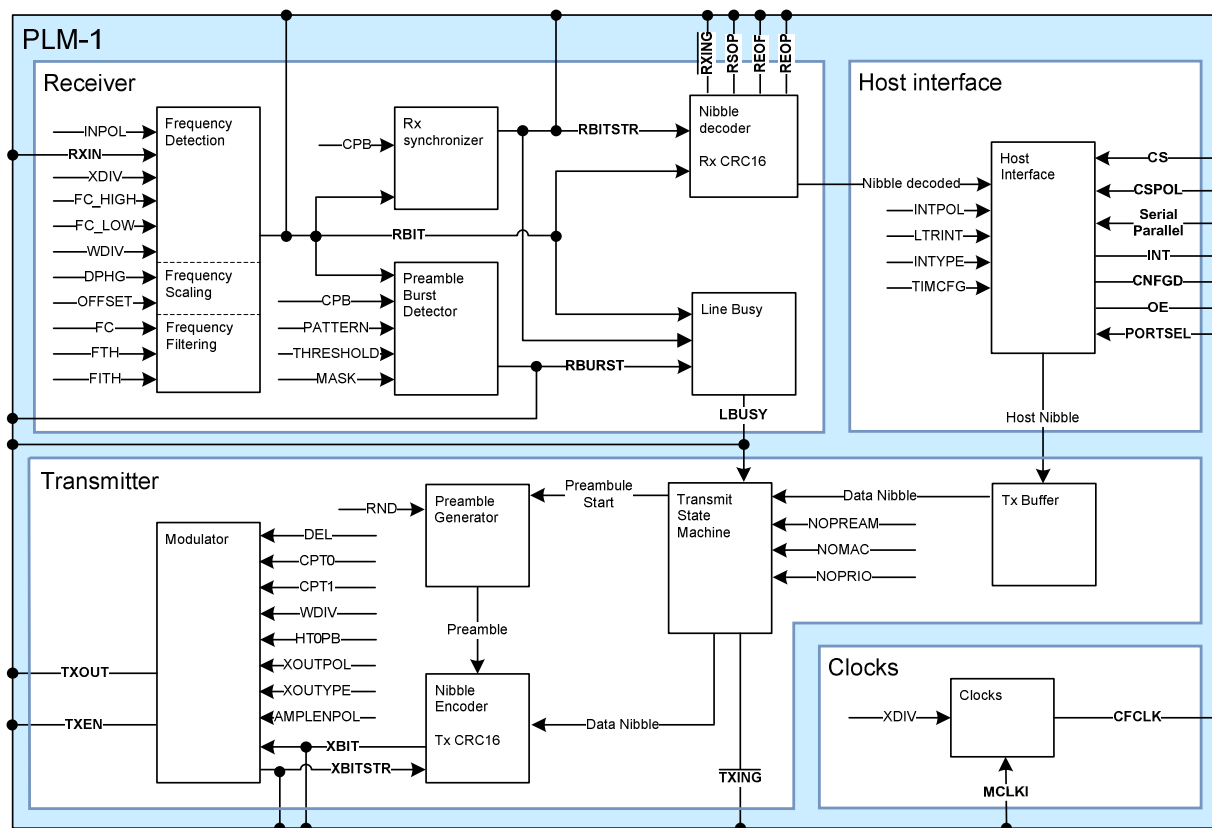


Figure 4-3 PLM-1 functional block diagram

### 4.3.2 Transmitter

This section first describes the steps performed by the host and the PLM-1 during a transmission. Then, configuration registers are explained from the functional block diagram perspective.

#### 4.3.2.1 Transmission Procedure

After a priority-queuing wait time defined by the first nibble of a packet, the PLM-1 automatically transmits a preamble in order to gain access to the channel. Then, it transmits a special internal character known as the Start of Packet, to notify receivers of the beginning of user data. It is followed by the transmission of the first nibble, to which error correction codes are automatically appended. Once the transmission of a data nibble starts, an interrupt is generated to the host to get the next nibble to transmit. User data is terminated by the End of Packet nibble, after which is automatically transmitted the CRC-16 value calculated internally during the entire transmission process. Figure 4-4 presents the internal transmission procedure handled by the Transmitter. This procedure is started by reading a data nibble from the host.

##### 4.3.2.1.1 First Nibble

The first nibble of a packet defines its priority. The PLM-1 analyses the first nibble of a packet and extracts priority information. The priority of a packet translates as a variable delay before transmission.

This function of the first nibble is disabled if using configuration option NOPRIO. Section 7.1 provides a technical description of the first nibble.

##### 4.3.2.1.2 Waiting for the Channel to be Available

From the moment it reads a nibble to transmit from the host, the PLM-1 waits for the channel to be available. Nothing is transmitted as long as the line is busy. Designers may choose to disable this function with the configuration parameter NOMAC, to be able to transmit even if the line is busy. This option should be used with caution. The status of the channel can be polled on **LBUSY** pin which is low when the channel is available and high when it is busy.

##### 4.3.2.1.3 Priority Queuing

In order to prevent nodes from keeping the channel constantly busy, the host sets a priority level to transmitted packets. Each priority level is associated with a time period the PLM-1 must wait before trying to gain access to the channel once it becomes available. Each packet can have a different priority, which is set through the first nibble of a packet. Priority queuing can be disabled with the NOPRIO configuration parameter.

The highest priority corresponds to 0s and the lowest corresponds to  $30T_b$  where  $T_b$  is the duration of a

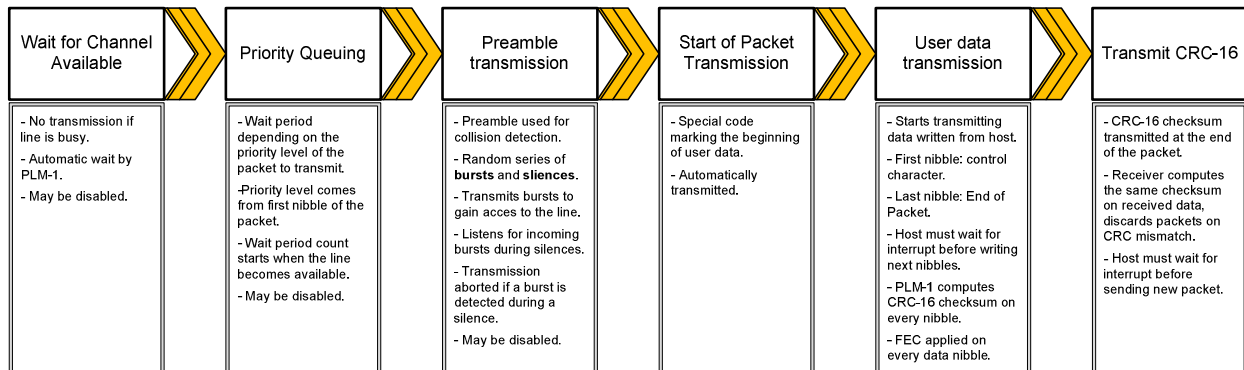


Figure 4-4 States of packet transmission by PLM-1

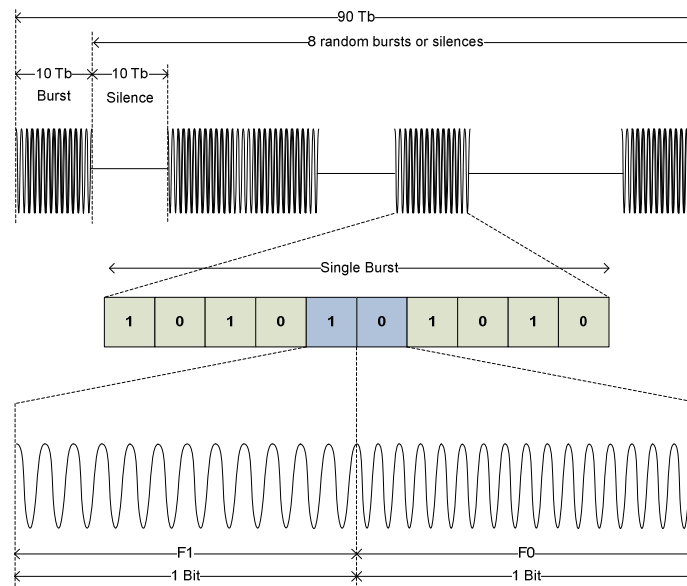


Figure 4-5 Decomposition of a preamble

bit. However, an extra delay of  $10T_b$  is added to the current priority if the modem was the last one to gain access to the communication channel. If the option NOPRIO is used, the extra delays is also disabled.

Detailed information on setting the priority can be found at Section 7.1.

#### 4.3.2.1.4 Preamble Transmission

Being half-duplex, the PLM-1 features a CSMA/CD algorithm to prevent devices from transmitting simultaneously. A preamble made of random **signal bursts** and **silences** is transmitted at the beginning of each packet to warn other nodes that a transmission is about to take place.

During silences, the medium is monitored by the receiver block, and a Collision is declared if the receiver detects a burst coming from another node. In this case, transmission is aborted and can be restarted once the channel becomes available again. If the preamble transmits without collision, the PLM-1 goes into Transmitting state and the TXING output activates.

When using master-slave protocols, preamble transmission can be disabled and achieve a slightly higher throughput. This is done with the NOPREAM configuration parameter.

#### 4.3.2.1.5 Start of Packet

PLM-1 data transmission is packet-oriented. At the PHY level, transactions are encapsulated within packet frames beginning with a Start of Packet internal character and ending with the End of Packet nibble. The Start of Packet is generated automatically right before transmitting the first data nibble of a packet. Therefore, the host never has to handle it.

#### 4.3.2.1.6 User Data

The PLM-1 transmits packets in a continuous flow of  $f_0$  and  $f_1$  frequencies. Since the PLM-1 Transmission Buffer holds user data one nibble at a time, the host has to wait between data nibble writes. When the PLM-1 starts the transmission of a nibble, it generates an interrupt which notifies the host that the next nibble is needed. This next nibble must be written before the current nibble transmission is over. If it fails to do so, the transmission is aborted and an error code is returned to the host.

**4.3.2.1.7 End of Packet**

The host terminates a packet by writing an End of Packet nibble to the PLM-1. After transmitting the End of Packet, the PLM-1 automatically transmits the CRC-16 value that was calculated internally throughout the packet, and the transmission terminates.

**4.3.2.2 Transmitter Block**

The Transmitter features a data buffer that holds nibbles to transmit. It feeds the Transmission State Machine, which manages priority queuing, preamble generation and packet transmission. It directly controls the Preamble generator, which generates random preamble preceding packet transmissions, and the Nibble Encoder, which applies the FEC and computes the CRC-16 on transmitted data. It also feeds the Modulator with bits to modulate (**XBIT**). The Modulator outputs the modulated signal (**TXOUT**) and a Transmitter Enable (**TXEN**) signal. It also outputs **XBITSTR**, a strobe signal which indicates when a bit transmission is complete.

**4.3.2.2.1 Transmission Buffer**

The transmitter block gets in function when the host writes a data nibble to the PLM-1. This nibble first goes in the Transmission Buffer, a temporary register that can hold one nibble. During transmission, an interrupt is generated to the host when the buffer is empty.

**4.3.2.2.2 Transmission State Machine**

From the moment the Transmission Buffer is not empty, the Transmitter State Machine evaluates the conditions for transmitting a packet. It waits for **LBUSY** to be inactive, showing the line is available.

**4.3.2.2.3 Preamble Generator**

The Preamble Generator is used when the configuration parameter **NOPREAM** is 0. A random number generator outputs the preamble envelope, setting the positions of the bursts and silences, as shown in Figure 4-5. Configuration register **RND** is the seed used by the random number generator.

Using different **RND** values for each node is recommended in applications that use intensively the collision detections. Otherwise, identical **RND** values can be used without concern.

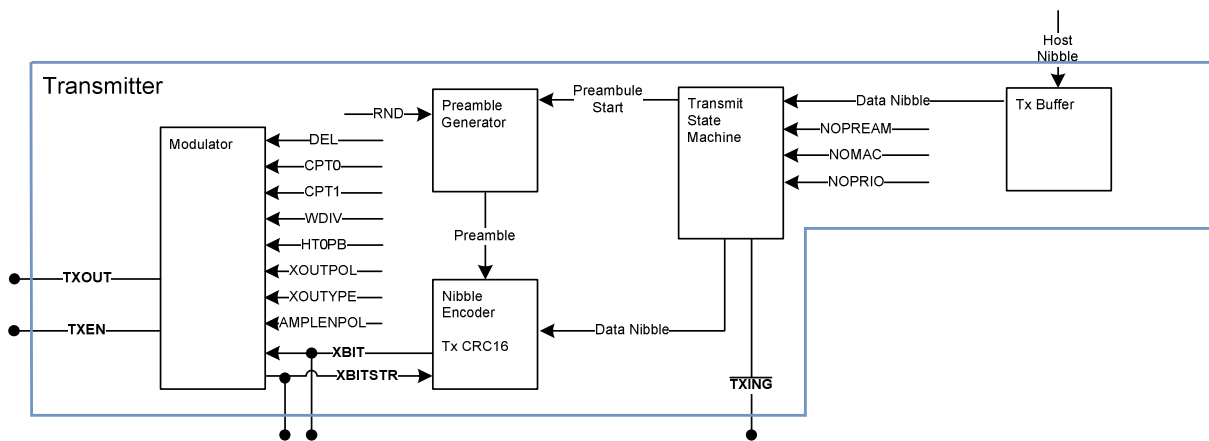


Figure 4-6 Transmitter functional block diagram

#### 4.3.2.2.4 Nibble Encoder

The Nibble Encoder takes data nibbles to transmit, converts them to FEC-encoded symbols before feeding them to the Modulation block. It also computes the CRC-16 value on each data nibble. This value is transmitted after the End of Packet for error detection purposes at the receiver.

While the encoding method is beyond the scope of this document, Table 4-2 shows supported nibbles and their equivalent FEC-encoded symbol. Encoded symbols are transmitted lsb first. It can be noticed that the Start of Packet not only has 22 bits, but it does not have any equivalent data nibble. This is because it has been selected to be unique and to eliminate the probability of detecting one within a data packet.

The output of this block is signal **XBIT**, which represents the bit being currently transmitted. This signal is only valid when output **TXEN** is active.

#### 4.3.2.2.5 Modulator

The frequency-shifting properties of the PLM-1 are obtained by mixing the reference clock  $f_{ref}$  alternatively with two lower frequencies  $\Delta f_0$  and  $\Delta f_1$ . Modulation frequencies  $f_0$  and  $f_1$  are obtained from these values in Equations (1) and (2).

Internal frequencies  $\Delta f_0$  and  $\Delta f_1$  can be obtained by dividing  $f_{ref}$  by two integers  $N_0$  and  $N_1$ :

$$\Delta f_0 = \frac{f_{ref}}{N_0} \tag{6}$$

$$\Delta f_1 = \frac{f_{ref}}{N_1} \tag{7}$$

Data nibble Hex	Encoded symbol (msb transmitted first)
0	01011100101
1	11110100101
2	11000011110
3	01101011110
4	01100011011
5	11001011011
6	11100001111
7	01001001111
8	00010101010
9	10111101010
A	10010111110
B	00111111110
C	00110111011
D	10011111011
E	10110101111
F	00011101111
End of Field (10)	11011110001
End of Packet (11)	01110110001
Start of Packet	00000000000 01111110100

Table 4-2 Nibble encoding table

Configuration registers CPT0 and CPT1 are used to express values  $N_0$  and  $N_1$  within the PLM-1.

$$CPT0 = N_0 - 2 \tag{8}$$

$$CPT1 = N_1 - 2 \tag{9}$$

Figure 4-7 presents the modulated output signal at pin **TXOUT** in relation to the bit that is being transmitted, which can be monitored on **XBIT**. The output signal is based on **CFCLK**, a clock of frequency  $f_{ref}$ , along with  $\Delta f_0$  and  $\Delta f_1$  in a configuration in which  $N_0 = 10$  and  $N_1 = 6$ . When a 0 is being transmitted, **TXOUT** gets inverted every  $\Delta f_0$  transition. When a 1 is being transmitted, **TXOUT** gets inverted every  $\Delta f_1$  transition.

4.3.2.2.5.1 Data Rate

The minimum bit period of a PLM-1 FSK configuration corresponds to the minimum time between two simultaneous edges of  $\Delta f_0$  and  $\Delta f_1$ . On Figure 4-7 it can be noticed that edges of  $\Delta f_0$  and  $\Delta f_1$  are synchronized both at point "a", which identifies the beginning of a bit period, and again at point "b", that corresponds to the end of a bit period.

Thus, the maximum data rate  $f_{bmax}$  can be calculated as follows:

$$f_{bmax} = \frac{f_{ref}}{CPB}, \tag{10}$$

where CPB is a configuration register of the PLM-1. It is computed externally as the Least Common Multiple of  $N_0/2$  and  $N_1/2$ . Values of CPB that are smaller than 18 are not recommended. In these cases, CPB can be doubled until its value is greater or equal to 18.

Configuration parameter WDIV can be used to divide the data rate by a power of 2. Its default value is 0 and its impact on the data rate  $f_b$  is expressed in the following equation.

$$f_b = \frac{f_{ref}}{2^{WDIV} CPB} \tag{11}$$

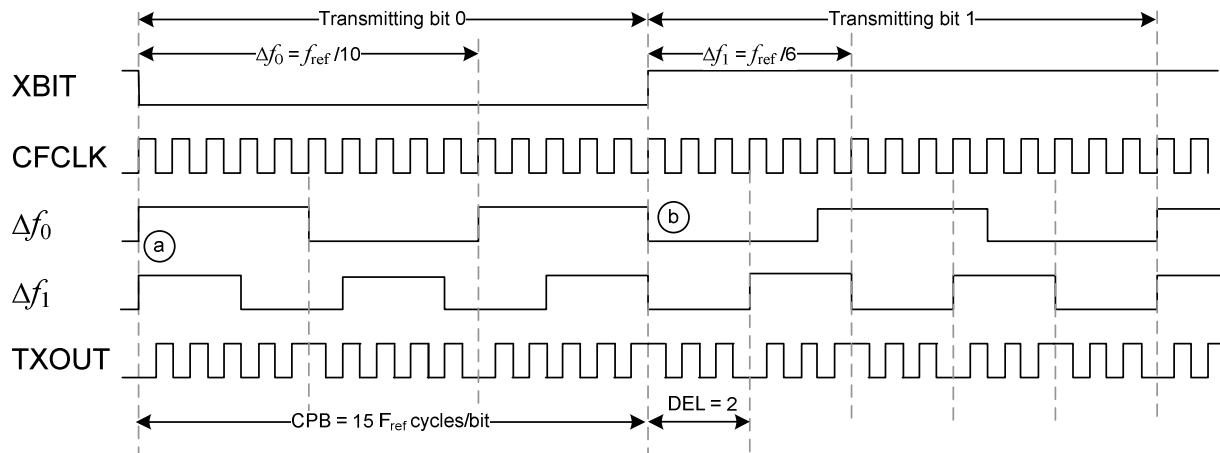


Figure 4-7 Example of PLM-1 modulation produced by phase inversions

In the modulator block, the data rate is expressed by two configuration registers: WDIV and HT0PB. The parameter HT0PB is directly related to CPB; it represents the number of transitions of  $\Delta f_0$  during the course of one bit.

$$HT0PB = \frac{2CPB}{N_0} - 1 \tag{12}$$

#### 4.3.2.2.5.2 Frequency transition acceleration

When the data signal to be modulated shifts from 1 to 0 or vice versa, the output of the external filter requires a certain time to shift from frequency  $f_0$  to  $f_1$ . This delay may limit the reception capabilities when using configurations with high data rates. This shift time limitation in the transfer rate of the filters can be improved by imposing a small delay before the first transition of the  $\Delta f_1$  signal. This configuration parameter called DEL is expressed as a number of  $f_{ref}$  cycles and its smallest value is 0, which sets the first transition of  $\Delta f_1$  at the first **CFCLK** rising edge during the bit period. Equation (13) shows the range of values DEL can take. Its default value is CPT1/2.

$$0 \leq DEL \leq \frac{CPT1}{2} \tag{13}$$

It should be noted that setting DEL to a small value may decrease the reliability of communication. This parameter should be used only for fine tuning in higher data rate situations. Figure 4-8 illustrates the impact of the configuration parameter DEL.

### 4.3.3 Receiver Operation

The receiver block is always active, except while the modem is transmitting. It constantly monitors the line to detect preamble bursts and verifies if the line is busy. It continuously synchronizes with incoming data and waits for a Start of Packet symbol before transferring demodulated, error-corrected data to the host. At the end of the packet, determined by the End of Packet, the CRC-16 nibbles confirm the success of the reception.

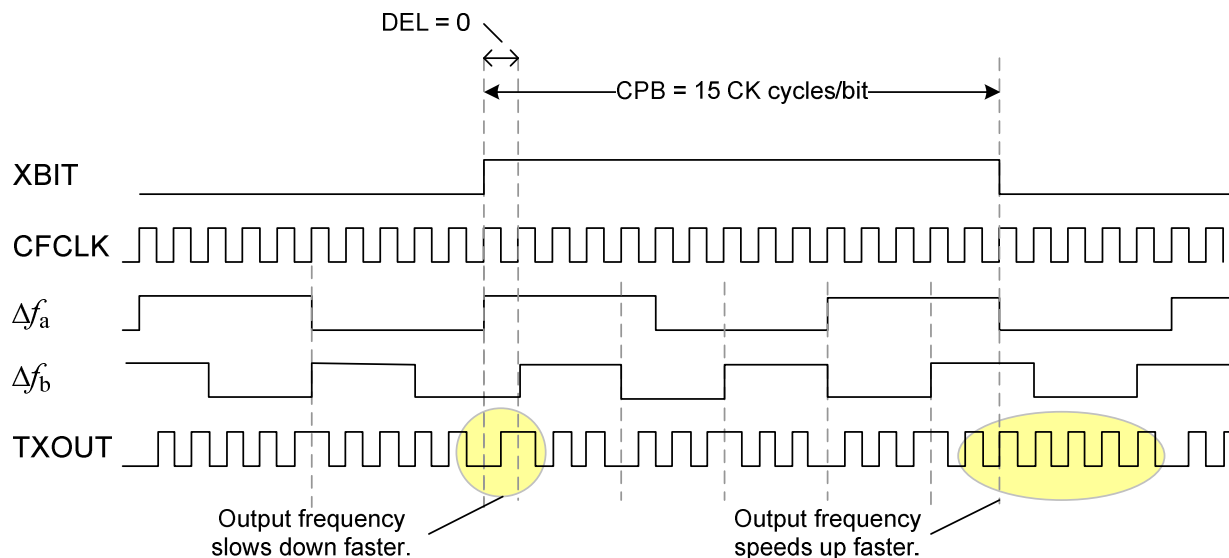


Figure 4-8 Smaller DEL values accelerates the transition from one frequency to the other

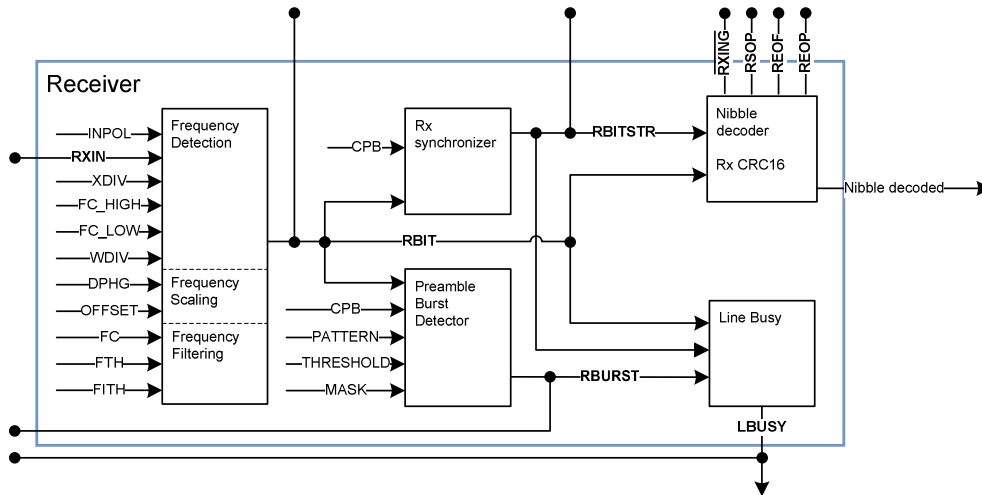


Figure 4-9 Receiver block diagram

### 4.3.3.1 Demodulation

The signal to demodulate is present at **RXIN** pin. Before any processing, configuration register INPOL specifies whether to perform the demodulation operations on the rising edge or on the falling edge of **RXIN**. The INPOL value should match the topology of the Analog Front-End Rx circuit.

#### 4.3.3.1.1 Frequency Detection

The first step of demodulation is performing rapid frequency measures of **RXIN** and compare them to  $f_{ref}$ . High and low frequency limits are used as a first means to eliminate unwanted frequencies. In order to keep this first demodulation stage from providing extreme values to the next stages, the receiver limits high frequencies defined by FC\_HIGH to  $1.5 f_{ref}$  and low frequencies defined by FC\_LOW to  $0.5 f_{ref}$ . The values of FC\_HIGH and FC\_LOW are presented in the following equations.

$$f_{Lim} = \frac{f_{osc}}{FC\_LOW} \tag{14}$$

$$f_{Hlim} = \frac{f_{osc}}{FC\_HIGH} \tag{15}$$

See default values of FC\_HIGH and FC\_LOW below.

$$FC\_LOW = \frac{f_{osc}}{2XDIV} \tag{16}$$

$$FC\_HIGH = \frac{3f_{osc}}{2XDIV} \tag{17}$$

The parameter WDIV can be used to divide the data rate by  $2^{WDIV}$ . Its default value is 0. Changing its value does not have any impact on parameters previously presented.

#### 4.3.3.1.2 Frequency Scaling

The Frequency Detection stage provides a raw snapshot of the received frequency at **RXIN**. The scaling stage allows formatting this data before applying a low-pass filter. Data is scaled to standardize digital

representations of frequencies from any configuration. Scaling is done by simply multiplying data by a power of 2, and adding an offset.

The gain and the offset are defined respectively by configuration registers DPHG and OFFSET, presented in the following equations.

$$DPHG = \left\lfloor \log_2 \left( \frac{2^{4-WDIV}}{XDIV} \frac{(N_0 \pm 1)(N_1 \pm 1)}{|N_0 - N_1|} \right) \right\rfloor - 1 \quad (18)$$

$$OFFSET = 2^{DPHG+WDIV+1} XDIV \frac{(N_0 \pm 1) + (N_1 \pm 1)}{(N_0 \pm 1)(N_1 \pm 1)} \quad (19)$$

Operator  $\pm$  should be replaced by '-' when  $f_0 = f_{L0}$  and  $f_1 = f_{L1}$ , and it should be replaced by '+' when  $f_0 = f_{H0}$  and  $f_1 = f_{H1}$ .

Please note that these equations are only given as a reference; **Ariane Controls provide software and firmware libraries which compute these parameters automatically.**

### 4.3.3.1.3 Frequency Filtering

Once it is scaled, a low-pass filter is applied on frequency information to convert the series of scaled raw snapshots into a smooth curve. Figure 4-10 presents the effect of the three stages of demodulation. First, raw frequency measurements are performed, and there is no large difference of values throughout the measured period. Each measured point is then scaled and centered around 0. When the values gets filtered, a smooth curve is obtained, showing the transition from one frequency to another as the filtered curve crosses zero. Signal **RBIT** is based on the sign of the filtered frequency data and represents the bit being received by the demodulator.

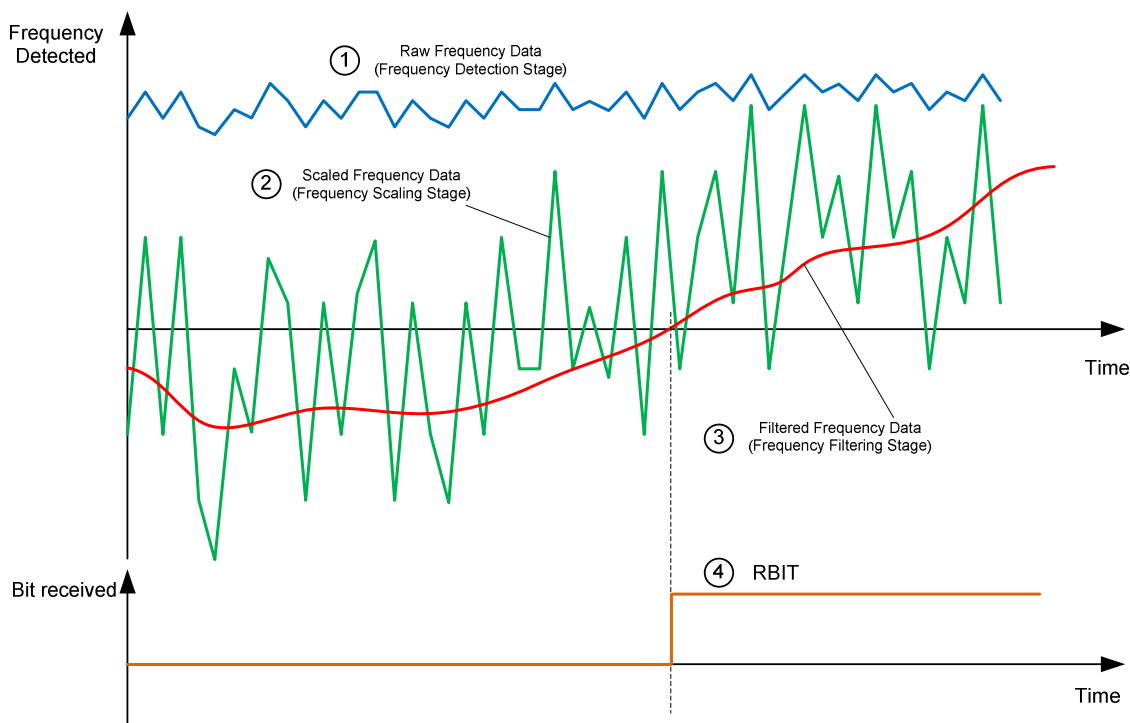


Figure 4-10 Example of raw, scaled and filtered frequency measurements used internally

The configuration parameter FC defines the cutoff frequency  $\omega_c$  of the filter. It is calculated from the desired time constant  $\tau$  of the filter. CPB/6 is used as the default time constant. The cutoff frequency is calculated as a 6-bit approximation of  $\omega_c$ .

$$\omega_c = \frac{1}{\tau} \quad (20)$$

The value of the time constant  $\tau$  selected being CPB/6, the cutoff frequency can be expressed as

$$\omega_c = \frac{6}{CPB}$$

$$\omega_c \approx \frac{15-m}{2^{n+4}}$$

where  $n$  and  $m$  are 3-bit integers computed as follows:

$$n = \lceil \log_2(\tau) \rceil - 1 \quad (21)$$

$$m = 15 - \lfloor 2^{n+4} \omega_c \rfloor \quad (22)$$

The parameter FC is then expressed:

$$FC = [n_2, n_1, n_0, m_2, m_1, m_0]$$

Its default value is tuned for optimal results.

The filtering stage also provides an invalid frequency threshold, as well as a filter clipping point, respectively called FTH and FITH.

Parameter FTH sets the frequency limit beyond which the filter output value is considered invalid by the next demodulation blocks. While one invalid bit received does not affect the demodulation process, receiving several invalid bits within a short period may abort the reception process.

FTH corresponds to a frequency called  $f_{FTH}$  and is calculated as follows.

$$FTH = 2^{DPHG+WDIV+2} \left[ XDIV - \frac{f_{osc}}{f_{FTH}} \right] + OFFSET \quad (23)$$

The default value of  $f_{FTH}$  is the upper limit of the FSK signal passband:  $f_0 + f_b$ .

Parameter FITH, associated to frequency  $f_{FITH}$ , sets the filter output clipping point. It is used to limit the range of the filter output. Its default value is  $2(FTH)$ .

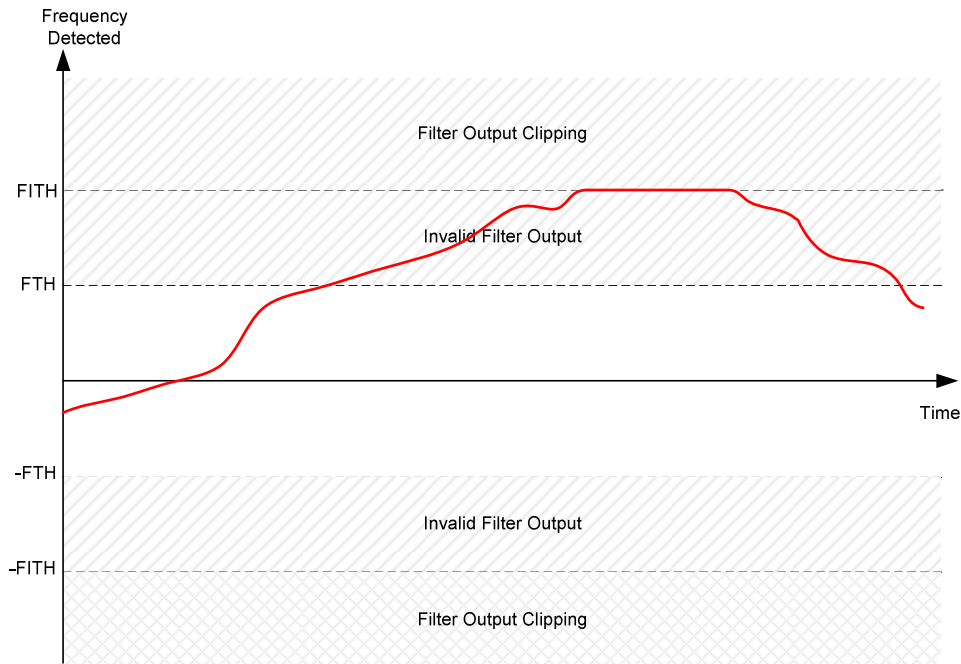


Figure 4-12 - The PLM-1 internal filter clips its output at frequency defined by FITH

#### 4.3.3.2 Receiver Synchronizer

The Receiver Synchronizer gets the received bit **RBIT** at its input and evaluates the moment to read a bit value. This moment, which depends on the internal filter FC parameter, is provided by **RBITSTR**. This signal generates a pulse every bit period or so, depending on how the modem is synchronized. The PLM-1 reads the **RBIT** signal every falling edge of **RBITSTR**. Usually, a demodulator synchronized to incoming packets generates **RBITSTR** pulses in the middle of bit periods. The example on Figure 4-11 shows the relation between **RBIT**, **RBITSTR** and the bit read by the demodulator.

#### 4.3.3.3 Nibble Decoder

Based on **RBIT**, **RBITSTR**, the bit value and a pulse showing the moment to read it, the Nibble Decoder waits to detect a Start of Packet and then begins to assemble data nibbles from bits received. This block also performs error correction through the PLM-1 FEC algorithm, and calculates a CRC-16 to detect corrupted packets. Decoded and corrected data nibbles are then transferred to the Host Interface, which transfers them to the host.

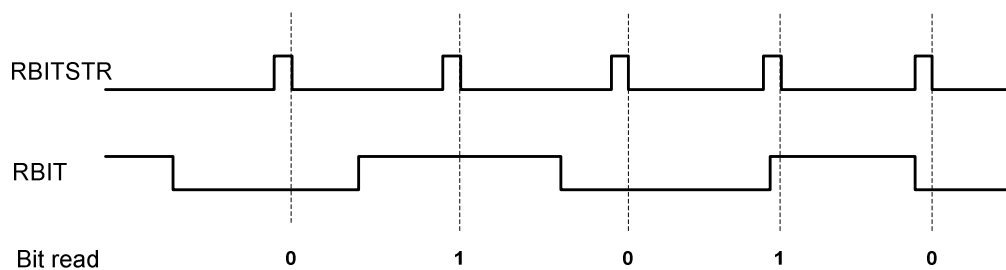


Figure 4-11 RBITSTR indicates when the RBIT value is sampled

### 4.3.3.3.1 Error correction

Considering the 11-bit encoded nibble H, the FEC algorithm will correct up to two bits in each nibble. We can express H as a bit array  $\{H_{10..0}\}$ . For each 11-bit symbol, the FEC algorithm can simultaneously correct 1 even bit ( $H_0, H_2, H_4, H_6, H_8, H_{10}$ ) and 1 odd bit ( $H_1, H_3, H_5, H_7, H_9$ ). The PLM-1 was designed so that 2 consecutive erroneous bits can be corrected.

### 4.3.3.3.2 CRC-16

If under any circumstance, the FEC algorithm is ineffective, the CRC-16 at the end of the packet will detect the error and the Nibble Decoder will transfer an error code to the host. The CRC-16 is completely handled by the PLM-1.

### 4.3.3.4 Line busy

The Receiver features a block that determines whether the line is busy. The line is busy when transmitting, receiving, or when there is constant noise in the communication pass band. The PLM-1 cannot start a transmission if the line is busy. If trying to start a transmission nibble while the line is busy, the PLM-1 will wait for the line to be available before transmitting a preamble. The status of the channel can be polled on **LBUSY** pin. The line also becomes busy as soon as a Preamble Burst is detected.

### 4.3.3.5 Preamble Burst Detector

The Preamble Burst Detector evaluates a sequence of frequency samples and generates a negative pulse on **RBURST** when it detects a preamble burst. It is used to control the access to the communication channel. In transmission, Collisions are triggered by the detection of a burst.

Burst detection can be tuned according to application conditions. It can be made more sensitive, which will slightly increase the efficiency of the Collision detection, but on the other hand may detect bursts from noise at the PLM-1 input. Burst detection also can be made less sensitive, thus reducing the chances of detecting bursts out of noise.

#### 4.3.3.5.1 Burst Bit Detection

While bits are usually determined by the state of **RBIT** when **RBITSTR** is active, burst bits are detected using another method, since bursts occur when the receiver is not yet synchronized to the incoming packet.

In burst decoding, every bit period is divided in a number of windows WPB which depends on CPB. WPB is *not a configuration parameter*; it is calculated internally by the PLM-1 and it can have values from 8 to 16.

Considering the 10-bit integer  $CPB_{9..0}$ , and supposing its most significant non-zero bit is  $CPB_n$ , the value of WPB is obtained by adding bit  $CPB_{n-4}$  to the 4-bit integer made from  $CPB_n$  and the 3 preceding bits.

$$WPB = \{0, CPB_n, CPB_{n-1}, CPB_{n-2}, CPB_{n-3}\} + CPB_{n-4}$$

To detect a burst bit, every bit period is divided into WPB windows. A sample of **RBIT** is taken for each window.

From this set of samples, updated every  $T_b/WPB$  seconds, a bit value is determined, based on configuration parameter THRESHOLD, which determines the bit detection bias.

Burst bit detection with low bias requires a large majority of identical bits in order to detect a burst bit. Alternatively, bit detection with high bias can tolerate many different bits and still detect a bit.

The minimum value of THRESHOLD is 0 (low bias) and its maximum value is WPB (high bias).

The default THRESHOLD value is  $WPB/2$ . The bias can be lowered when many collisions are detected in transmission. Lowering the THRESHOLD value will then tighten bit detection decisions, thus decreasing the number of collisions.

The bias can be increased in applications that require a great sensitivity to preambles. In these cases, increasing the THRESHOLD value will loosen bit detection decisions, and bursts will be detected more often.

Most of the time, the default THRESHOLD value is appropriate and does not need tuning.

#### 4.3.3.5.2 Burst Detection

A preamble burst is the fixed 10-bit value 2AAh. A Burst can be detected from a subset of these bits. The Preamble Burst Detector provides a configurable method of detecting bursts without using the RBITSTR signal. Instead of one bit reading for each bit period, the Burst Detector takes WPB bit readings during one bit period. All these readings are kept in memory for 8 bit periods.

In addition to parameter THRESHOLD, used for bit detection, two other configuration parameters are used for Burst recognition: PATTERN and MASK.

PATTERN determines the pattern of a burst in reception. Since in transmission a burst corresponds to 2AAh, the recommended PATTERN value is AAh, but value 55h can be used as well.

Also, the parameter MASK is a logic mask which can disable the verification of some bits, in order to adjust Burst detection sensitivity. The default MASK value is FCh. It is recommended to set MASK to a value with at least 4 contiguous 1 to ensure reliable Burst detection.

MASK value	Comments
FCh	Default MASK value. FCh = 11111100b. Six consecutive PATTERN bits must be detected in order to declare a Burst reception.
FFh	FFh = 11111111b. Eight consecutive PATTERN bits must be detected in order to declare a Burst reception. This MASK value makes Bursts more difficult to detect, leading to less collisions.
F0h	F0h = 11110000b. Four consecutive PATTERN bits must be detected in order to declare a Burst reception. This MASK value makes Bursts easier to detect, leading to more collisions, but increasing the efficiency of the CSMA/CD algorithm, i.e. Bursts are detected sooner, more often.

Table 4-3 Example of MASK values

### 4.3.4 Host Interface

The Host Interface block manages communications with the host. It features many complementary functions. It can be configured through 4 parameters, three of which are related to the **INT** pin, while the other controls the internal Timer function.

#### 4.3.4.1 Interrupt configuration

The interrupt polarity can be configured through parameter **INTPOL**. If **INTPOL** = 0, the **INT** pin is active low and if **INTPOL** = 1, then it is active high.

When idle, the **INT** pin can be configured to be either in high-impedance state or in logic state. Parameter **INTYPE** controls the state of **INT** while it is inactive. If **INTYPE** is 0, **INT** is in high-impedance state while inactive. If **INTYPE** is 1, **INT** will be in logic state while inactive.

Finally, parameter **LTRINT** determines when the **INT** signal goes inactive. When **LTRINT** is 0, the **INT** pin goes inactive when the parallel port strobe or the SPI serial clock activates. This is why the parallel port strobe must always be set to 0 when inactive. If **LTRINT** is 1, the **INT** pin is reset when the PLM-1 has completely transferred.

#### 4.3.4.2 Internal Timer

The PLM-1 features an internal Timer that can generate periodic interrupts. The basic time unit of the timer is a bit period  $T_b$ . Configuration parameter **TIMCFG** determines the number of bit periods between each interrupt. It holds an 8-bit value, so the maximum timer interval is  $255T_b$ .

The timer can be started with control nibble **STRT** and stopped with control nibble **STOT**.

## 5 Configuration Parameters

The PLM-1 offers great flexibility when it comes to communication frequencies, data rate, MAC configuration and hardware interfacing. The key to this flexibility lies in the several configuration parameters described in this section.

The PLM-1 configuration parameters can be divided into three categories: communication, MAC and hardware interface. This section presents the use of each parameters. For more details, Section 0 provides a detailed description of each parameter with respect to the internal operation of the chip.

These parameters are packaged into a nibble array and written to the PLM-1 after power-up. Only then does it start to operate. This Initialization sequence is detailed in Section 0.

### 5.1 Communication Parameters

The configuration parameters related to the communication define the FSK frequencies, the data rate, and various modulation and demodulation characteristics of the transceiver. These parameters can be divided into two groups: Basic and Advanced. Basic parameters are selected by the user and define essential information for the modulator and demodulator operation. Values of these parameters can be obtained in different ways. Appendix A of this document provides several examples of basic communication parameters based on communication frequencies and data rates. These parameters also can be determined using Ariane Controls' ACES software.

Advanced communication parameters are usually left to their default values, which are optimized for our reference designs and typical line conditions. These default values are computed automatically by firmware libraries or by the ACES software. Users wanting to modify these values are invited to read Section 0 on Advanced internal operation.

The communication frequencies and data rate are computed solely based on the four basic configuration parameters and the external clock frequency  $f_{osc}$ .

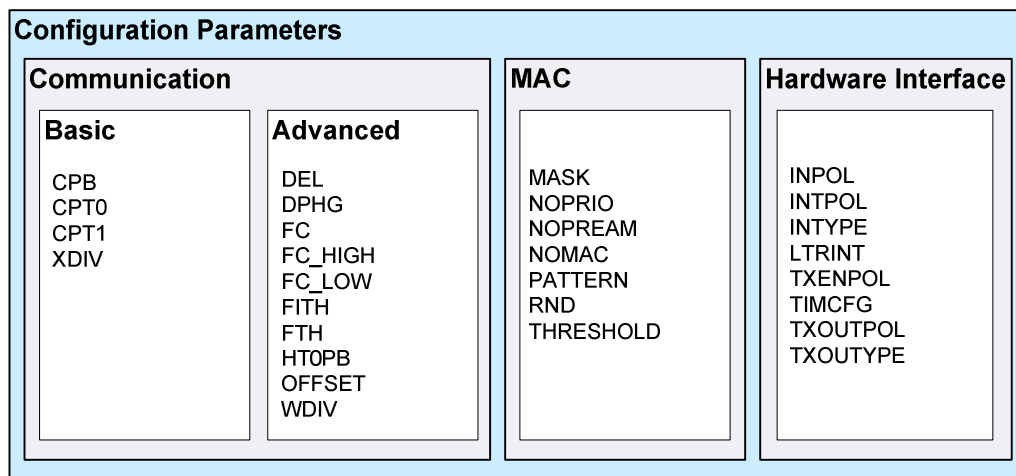


Figure 5-1 PLM-1 Configuration parameter categories.

### 5.1.1 Basic Communication Parameters

There are four Basic communication parameters. Each of them defines important parts of the PLM-1 FSK modulation, presented in Figure 4-1 on page 16.

#### **XDIV** [7 bits]

The reference frequency  $f_{ref}$  is obtained by dividing the **MCLKI** frequency  $f_{osc}$  by configuration parameter XDIV. The reference frequency is used as an anchor point for communication frequencies. The reference frequency can be monitored at pin **CFCLK**.

#### **CPTn** [8 bits]

Communication frequencies are obtained by mixing  $f_{ref}$  with slower frequencies  $\Delta f_0$  and  $\Delta f_1$ , as stated in Equations (1), (2), (3) and (4). Configuration parameters CPT0 and CPT1 are used to define  $\Delta f_0$  and  $\Delta f_1$  so the PLM-1 can generate the appropriate frequencies.

$$\Delta f_n = \frac{f_{ref}}{CPTn+2} \quad (24)$$

Small CPTn values generate frequencies that are far from  $f_{ref}$ , and therefore easier to filter, which lead to better performances in reception.

#### **CPB** [10 bits]

The last basic communication parameter is related to the data rate. The parameter CPB defines the maximum data rate  $f_{bmax}$  by specifying the number of  $f_{ref}$  cycles during one bit. By looking at Equation (10) on page 24, it can be seen that the maximum data rate only depends on  $f_{ref}$  and CPB. As shown in Figure 2-2, the maximum data rate increases as communication frequencies increase, or as CPB decreases. However, CPB cannot get values lower than 15.

In harsh power line environments, lower data rates will generally provide better reliability.

### 5.1.2 Advanced Communication Parameters

Advanced communication parameters are usually left to their default values computed by firmware libraries or software.

#### **DEL** [7 bits]

The DEL parameter controls the rapidity of transition from a frequency to the other. Decreasing this value will accelerate frequency transitions. It should be modified with care, and only when using high data rate configurations.

#### **DPHG** [4 bits]

During the demodulation procedure, raw data representing the detected frequency is scaled by a gain and an offset. The gain is defined by DPHG, which represents a power of 2. Its value should not be modified. For more details, see Section 4.3.3.1.2.

#### **FC** [6 bits]

The PLM-1 receiver integrates a digital low-pass filter used to correlate received frequencies to the bit received. The cutoff frequency of this filter is represented by FC, a 6-bit integer. Its default value is adjusted so the received bit is identified after about 30% of the bit period. Section 4.3.3.1.3 provides details about the format of the parameter and the default value computation. Increasing the FC will increase the bit transition time in reception, whereas decreasing it will have the opposite effect. It is recommended to always use the default value.

**FC\_HIGH** [8 bits]

At the beginning of the demodulation stage, a mechanism blocks frequencies that are greater than the frequency defined by FC\_HIGH. This frequency can be obtained from Equation (15).

**FC\_LOW** [8 bits]

At the beginning of the demodulation stage, a mechanism blocks frequencies that are lower than the frequency defined by FC\_LOW. This frequency can be obtained from Equation (14).

**FITH** [8 bits]

The demodulator provides the possibility to configure the range of frequencies it processes. This range is defined by FITH. The default range depends on the configuration bandwidth B:

$$B = 2f_b + f_0 - f_1$$

Using default values, the PLM-1 processing limit frequencies correspond to  $f_c \pm B$ . For more details, see Section 4.3.3.1.3.

**FTH** [7 bits]

Parameter FTH determines the range of frequencies that are considered valid internally. If the external filtering does not provide adequate attenuation outside the passband, it may be helpful to decrease the FTH and FITH values so that only frequencies near  $f_c$  are being considered for demodulation. However, doing so may reduce the robustness of the demodulation. Using narrow external filters in reception remains the best design approach. The default FTH value translates to a range that has limits of  $f_c \pm B/2$ . Technical details are available in Section 4.3.3.1.3.

**HT0PB** [5 bits]

This value is closely related to CPB, it represents the number of  $\Delta f_0$  half-cycles during one bit. Always use the default value. As a reference, HT0PB can be obtained from Equation (12) in Section 4.3.2.2.5.1.

**OFFSET** [11:0]

This configuration parameter is used along with DPHG for scaling data during demodulation. Its value is added to each data sample previously scaled with DPHG. Always use the default value, calculated in Section 4.3.3.1.2.

**WDIV** [2 bits]

While CPB is used to calculate the maximum data rate, WDIV is used to reduce it by a factor of  $2^{\text{WDIV}}$ . Its default value is 0. When modifying WDIV, DPHG must be modified as well. This is done automatically by the Ariane Controls software and firmware libraries.

## 5.2 MAC Parameters

Configuration parameters can be used to tune the medium access controller of the PLM-1. These include the preamble generation and detection, the packet types and the priority levels.

The preamble used for line contention is made of **bursts** and **silences**. Bursts are 10-bit symbols transmitted to warn other nodes that it is about to transmit data. During silences, the PLM-1 monitors the channel and detects incoming bursts. If an incoming burst is detected during a preamble silence, a collision occurs and the transmission is aborted. Burst detection, on which the CSMA/CD strategy is based, can be configured according to the application.

**MASK** [7 bits]

This parameter determines which matching bits are used to recognize a preamble burst. The maximum number of bits is 8. For instance, if its value is 0Fh, only four bits of the burst symbol must be detected to

declare that a burst has been received. This leads to a more sensible detector that can trigger collisions more easily. It might even detect bursts out of noise in very harsh environments. However, if MASK is set to FFh, 8 bits of the burst must be detected in order to declare one. This leads to a more rigid correlation. The MASK default value is FCh, which is an optimal trade-off between sensitivity and robustness.

**NOMAC [1 bit]**

The **LBUSY** pin is high when the line is busy, e.g. when the receiver detects a signal or noise in the communication passband. By default, the PLM-1 waits for this signal to be low before starting any transmission. However, setting NOMAC to 1 disables this behaviour. This option should only be used in network designs using master-slave topology. The default NOMAC value is 0.

**NOPREAM [1 bit]**

Setting NOPREAM to 1 disables the preamble transmission. Like NOMAC, this disables the collision detection algorithm, so it should only be used in designs in which no simultaneous transactions are possible. The default NOPREAM value is 0.

**NOPRIO [1 bit]**

The first nibble of a packet has 2 reserved bits used for priority queuing. This restriction can be removed by setting NOPRIO to 1. In this case, every packet will be transmitted with highest priority and the 2 reserved bits can be used as ordinary data bits. Default NOPRIO value is 0.

**PATTERN [8 bits]**

A preamble Burst is an 10-bit symbol of alternating 1's and 0's. When detecting a burst, the 8-bit PATTERN specifies what pattern to detect. The default value is AAh and should not be changed.

**RND [8 bits]**

The preamble is a random set of bursts and silences. A random number is used for every preamble. Value RND is the seed of the random number generator. It is suggested to give RND different values for each node in applications that provide heavy solicitation of the CSMA/CD mechanism.

**THRESHOLD [5 bits]**

The THRESHOLD value defines the tolerance of burst detection. With high values, bursts are recognized easily and with smaller values, the PLM-1 adds more restriction to its burst recognition algorithm. Setting this value too high may have for effect to mistake incoming noise for bursts, thus creating a lot of collisions. Inversely, setting this value too low may make bursts too difficult to detect, sometimes resulting in failure of the CSMA/CD procedure. It is recommended to use the default THRESHOLD value.

**Reserved bits [2 bits]**

Parameters RSVB1 and RSVB2 are reserved. They must be set to 1 at all times.

### 5.3 Hardware Parameters

The PLM-1 offers a lot of flexibility regarding the hardware configuration. Parameters can modify the operation of the **INT** pin, as well as the polarity or default state of other I/Os.

**INPOL [1 bit]**

This parameter defines the polarity of the frequency detection synchronization of the **RXIN** pin. Depending on the output characteristics of the external sine-to-square-wave converter, the transition having the lowest response time should be selected. Possible values are 1 (rising edge) and 0 (falling edge), and the default value is 1.

**INTPOL** [1 bit]

The polarity of the interrupt pin can be configured through the **INTPOL** parameter. The default value is 1, which makes the **INT** pin active high, whereas a 0 makes it active low.

**INTYPE** [1 bit]

In absence of an interrupt, the **INT** pin of the PLM-1 can either be in high impedance state or in logical state. The value of **INTYPE** determines the idle state: 0 corresponds to a high-impedance idle state, 1 corresponds to a logic level idle state.

**LTRINT** [1 bit]

This parameter determines the interrupt mode of the PLM-1: Transition (or edge): 0, and Level: 1. These interrupt modes differ in the way the interrupt pin is reset. When using the Level mode, the **INT** pin is reset when the PLM-1 has completely transferred its outgoing data to the host. When using the Edge mode, the **INT** pin is reset when the **STRB/SCLK** pin activates to start a transaction. The default value is 0.

**TIMCFG** [8 bits]

The PLM-1 features an internal timer which, when activated, generates periodic interrupts. **TIMCFG** controls the timer interval period. Each unit correspond to one bit period. The default value is 11, which corresponds to the duration of a nibble.

**TXENPOL** [1 bit]

This value defines the polarity of the Enable pin of the operational amplifier used in transmission. The default value is 1 and corresponds to active high, whereas a 0 value corresponds to active low.

**TXOUTPOL** [1 bit]

This parameter defines the idle polarity of the pin **TXOUT**. For optimal results, this value should match the **INPOL** parameter.

**TXOUTYPE** [1 bit]

When this parameter is set to 0, the pin **TXOUT** is in a high impedance state when the modem is not transmitting. When set to 1, which is the default value, the **TXOUT** idle state is in logic level.

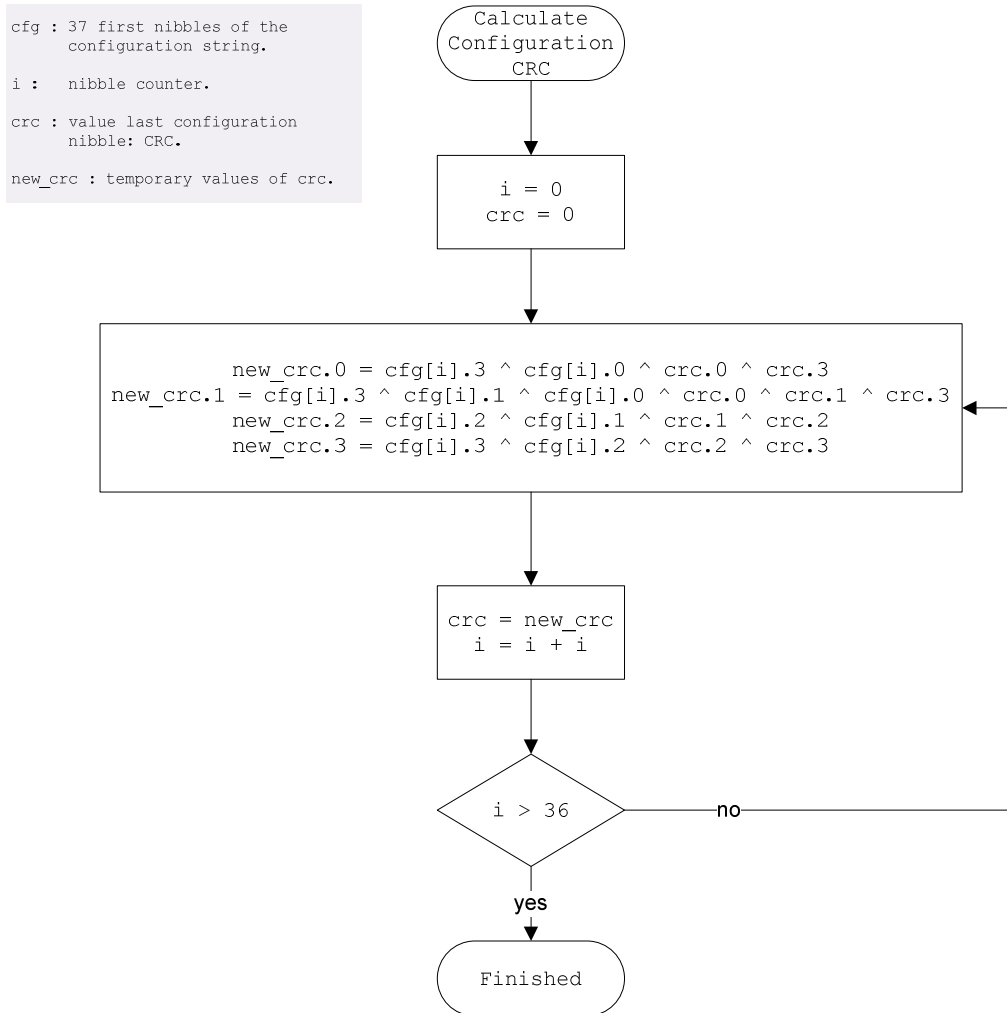


Figure 5-2 Calculation of configuration string CRC nibble

## 5.4 Initialization Sequence

All configuration parameters presented in the previous section have to be written to the PLM-1 to enable communication in the form of a 38-nibble sequence called *configuration string*. Table 5-1 presents the disposition of the configuration string nibbles in a byte array. After power-up or a reset, the host writes this array to the PLM-1, starting with the most significant bits of byte 0: PATTERN[7:4]. More details on interfacing the PLM-1 are provided in section 8.

### 5.4.1 CRC

The last configuration nibble is a CRC used to verify the integrity of the configuration string. If the configuration string is correctly written and the CRC is correct, the CNFGD pin goes high. The CRC value can be computed by the host firmware or by software. Firmware CRC computation is recommended since it allows designers to generate the configuration string automatically. Software tools and firmware libraries provided by Ariane Controls perform automatic CRC computation.

Configuration String							
0	PATTERN[7:0]						
1	MASK[7:0]						
2	THRESHOLD[4:0]				XDIV[6:4]		
3	XDIV[3:0]			DPHG[3:0]			
4	OFFSET[10:3]						
5	OFFSET[2:0]			FITH[7:3]			
6	FITH[2:0]			FTH[6:2]			
7	FTH[1:0]		FC[5:0]				
8	WDIV[1:0]	INPOL	LTRINT	INTPOL	INTYPE	XOUTPOL	XOUTYPE
9	TXENPOL	RSVB2	RSVB1	NOPRIO	NOPREAM	NOMAC	CPB[9:8]
10	CPB[7:0]						
11	DEL[6:0]						HTOPB[4]
12	HTOPB[3:0]			CPT1[7:4]			
13	CPT1[3:0]			CPT0[7:4]			
14	CPT0[3:0]			RND[7:4]			
15	RND[3:0]			TIMCFG[7:4]			
16	TIMCFG[3:0]			FC_LOW[7:4]			
17	FC_LOW[3:0]			FC_HIGH[7:4]			
18	FC_HIGH[3:0]			CRC[3:0]			

Table 5-1 Configuration string in a byte array

## 6 Control Codes

While the PLM-1 configured through the configuration string, it is operated with Control Codes. This section gives information about these codes, which are essential for packet transmission and reception.

### 6.1 Input Control Codes

Input control codes are used by the host to give commands to the PLM-1. These codes can be written to the PLM-1 at any time, except during configuration.

#### 6.1.1 End of Field – 10h (EOF)

The End of Field is a special data nibble that can be transmitted or received like any data nibble. Its usage is determined by the host application. This nibble is transmitted in data packets, along with the nibbles. An EOF may not be used as a packet's first nibble.

Writing 10h as a data byte to the PLM-1 during transmission will use this special field.

#### 6.1.2 End of Packet – 11h (EOP)

The End of Packet is a special nibble used to terminate a packet. This nibble indicates to the PLM-1 to append its internally-calculated CRC-16 to the packet. A packet may not be started with an EOP. After writing an End of Packet to the PLM-1, the host must wait until it read a Transmitter Register Empty control code before starting to transmit a new packet.

During transmission, writing 11h to the PLM-1 while the transmit register is empty releases the End of Packet symbol.

#### 6.1.3 Disable Receiver – 12h (DISR)

This output code is used to tell the PLM-1 to abort the reception of the current packet. At any time during a packet reception, 12h can be written and the reception will stop until a new packet is detected.

Code	Name	Abbreviation	Description
10h	End of Field	EOF	All-purpose special data nibble
11h	End of Packet	EOP	Used to terminate a packet
12h	Disable Receiver	DISR	The PLM-1 stops the transfer of the packet to the host until a new packet is detected.
13h	Reserved	RESERVED	Reserved for future use
14h	Start Timer	STRT	Starts free-running timer
15h	Stop Timer	STOT	Stops the free-running timer
16h	Soft Reset	RESET	Resets the chip
17h to 1Eh	Reserved	RESERVED	Reserved for future use
1Fh	No Operation	NOP	No Operation

**Table 6-1 PLM-1 input control codes**

#### 6.1.4 Start Timer – 14h (STRT)

The PLM-1 features an internal timer which generates interrupts at a rate specified by configuration TIMCFG. Writing code STRT (14h) starts this timer.

#### 6.1.5 Stop Timer – 15h (STOT)

The Stop Timer command stops the internal timer.

#### 6.1.6 Reset – 16h (RESET)

The PLM-1 modem can be reset by the host sending the command RESET (16h) through the communication port. By resetting the PLM-1, it loses its configuration and is ready to receive a new configuration string.

This operation can also be handled by driving the **RESET** pin low for at least  $8T_{osc}$ .

#### 6.1.7 No Operation – 1Fh (NOP)

The No Operation nibble is simply ignored by the PLM-1. This command must be used when reading data from the PLM-1 in SPI mode.

### 6.2 Output Control Codes

Output control codes are used by the PLM-1 to report its status to the host. When it has to transfer such codes, the PLM-1 asserts its interrupt line so the host can start a transfer on the communication port.

#### 6.2.1 End Of Field – 10h (EOF)

The End of Field is a special data nibble. It is received when the remote transceiver inserted one on the outgoing packet.

#### 6.2.2 End of Packet – 11h (EOP)

Reading an End of Packet marks the end of the packet currently being received, and indicates the internal CRC verification has been successful.

#### 6.2.3 Error Received – 12h (ERR)

The PLM-1 writes this code to the host when it has detected an error on a reception (e.g., wrong CRC, carrier is lost while receiving, FEC error). When this code is read, the host must abort the current packet reception.

#### 6.2.4 Receiver Over-Run – 13h (ROVR)

This nibble is received when the host took too much time (longer than about  $11 T_b$ ) before reading the last nibble during reception. When the PLM-1 has to write a data nibble to the host, an interrupt is generated. If the host doesn't read it in time, the PLM-1 overwrites the data nibble with a Receiver Over-Run code. Reception of the current packet is then aborted. The host may try to gain access to the channel for next packet transmission.

Code	Name	Abbreviation	Description
10h	End of Field	EOF	End of Field special nibble received.
11h	End of Packet	EOP	Packet received successfully.
12h	Error received	ERR	The received packet contains an error and should be discarded. Reception is aborted.
13h	Receiver Over-Run	ROVR	The chip over-wrote the receiver register because the host did not read the last value soon enough. Reception is aborted.
14h	Collision	COLL	Detected another transmission while contending for the channel. Transmission should be retried later.
17h	Transmitter under-run	TUNR	The host did not write transmission data soon enough after reading the last input code. Transmission is aborted.
18h	Transmit Register Empty	TXRE	The PLM-1 has gained access to the channel and requests the next data nibble of the outgoing packet..
19h	Transmitter over-run	TOVR	The transmitter did not read the last input nibble soon enough. Transmission is aborted.
1Ah	Timer Elapsed	TEL	Free-running timer elapsed.
1Bh	Timer over-run	TIMOVR	The PLM-1 over-wrote the timer before the host read the timer status.
1Ch to 1Eh	Reserved	RESERVED	Reserved for future use.
1Fh	No Operation	NOP	No Operation.

Table 6-2 PLM-1 output codes

### 6.2.5 Collision – 14h (COLL)

When the PLM-1 detects an incoming preamble while being in the process of transmitting a preamble, a collision is detected. This control nibble is then transferred to the host, and will usually be followed by data nibbles. Transmission should be restarted.

### 6.2.6 Transmitter Under-Run – 17h (TUNR)

A Transmitter Under-Run occurs during transmission when an interrupt with a TXRE is generated by the PLM-1 and the host fails to provide the next nibble for transmission within  $11 T_b$  since the interrupt rising edge. The transmission is then aborted. This code should not occur in normal operation.

### 6.2.7 Transmitter Register Empty – 18h (TXRE)

After the transmission of each nibble of a packet, an interrupt is generated with the TXRE code ready to be written to the host. Upon reception of this code, the host must immediately write the next nibble to be transmitted.

The frequency of these interrupts are function of the configuration data rate. The maximum time period between 2 TXRE interrupts is  $11 T_b$ , where  $T_b = 1/f_b$ .

After writing an EOP to the PLM-1, the host must wait for a TXRE code before transmitting the next packet. This last TXRE code confirms the internal CRC-16 has been appended to the packet and transmitted.

### **6.2.8 Transmitter Over-Run - 19h (TOVR)**

When the PLM-1 generates an interrupt with a TXRE code and the host does not read it in time, the Transmitter Over-Run code is returned and transmission is aborted.

### **6.2.9 Timer Elapsed - 1Ah (TEL)**

When the internal timer is started, an interrupt with control code TEL is generated every TIMCFG  $T_b$ .

### **6.2.10 Timer Overrun - 1Ah (TOVR)**

Once an interrupt with code TEL is generated, the host must read it before the timer reaches its limit a second time. Otherwise, code TOVR is released.

### **6.2.11 No Operation - 1Fh (NOP)**

The NOP control code should be written to the PLM-1 when using the SPI interface and performing a read operation.

## 7 Packet Format

The PLM-1 can use any protocol to transmit information. However, PLM-1 packets must comply with a standard header that can be added to the protocol frame, and must end by an End of Packet nibble. Also, the maximum packet size is limited to 63 bytes, or, more precisely, 127 nibbles.

### 7.1 First Nibble

The first nibble of a packet indicates the priority of the current packet. Four different priority levels are available: Highest, High, Normal and Deferred. Each priority level is associated with a time period that specifies the minimum time allowed between the end of a transmission/reception and the beginning of a transmission. The priorities and their respective delay are shown on Figure 7-1.

The format of the first nibble is shown in Figure 7-2. The three most significant bits are {0, 1, 0} and the two least significant bits define the priority of the packet.

The priority option can be disabled through the NOPRIO configuration register. Even in this case, the standard header should be used as well.

### 7.2 Channel

The second header byte is the channel number, which can get values from 1 to 255. Designers should select a channel number for their application to reduce the possibility of interfering with other networks.

Incoming packets should be parsed and discarded if the channel field does not match the channel selected for the application.

### 7.3 Addressing

The PLM-1 provides PHY and MAC layers, both of which do not support addressing. This task must be handled by the host. The protocol neutrality of the PLM-1 allows it to be easily adapted to many applications.

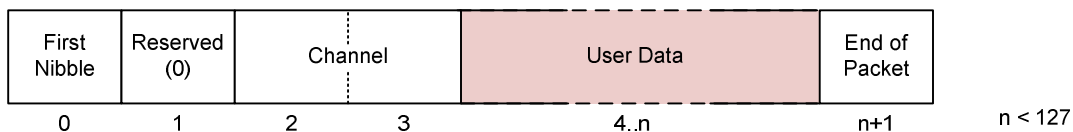
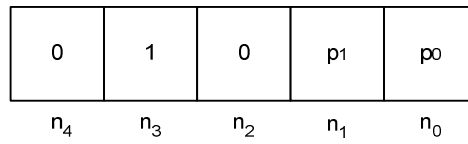


Figure 7-1 Structure of a PLM-1 n-nibble packet



First nibble	Priority bits [p1, p0]	Priority	Delay
01000	00b	Highest	0
01001	01b	High	$10 T_b$
01010	10b	Normal	$20 T_b$
01011	11b	Deferred	$30 T_b$

**Figure 7-2 The first nibble of a packet defines the type and priority of a transmission**

## 8 Interfacing with a CPU

This section describes the communication between the PLM-1 modem and a CPU, including the configuration string, supported packet format and control codes.

### 8.1 Host interface

The PLM-1 host interface provides two types of communication: serial (SPI) and parallel. In both modes, a master-slave design is used in which the PLM-1 acts as a slave. The **PORTSEL** pin enables the selection of the interface; the port is set in serial mode when the pin is low and in parallel mode when it is high. In either mode, the clock is provided by the host or by an external oscillator and data are synchronized internally to the **MCLKI** clock. Each time the PLM-1 has to transfer information to the CPU, the interrupt pin is asserted and remains so until the host reads the data. If the host has to read more than one set of data, the interrupt pin will stay asserted between readings.

The PLM-1 offers the following interfacing features:

- Serial and parallel mode
- Programmable clock polarity for serial mode
- Programmable Chip Select (**CS**) polarity
- Port and line status monitoring

The serial mode is SPI compliant and supports SPI clock frequencies up to  $f_{osc}/4$ . Table 8-1 shows the functionality of each pin of the port depending on the **PORTSEL** pin state.

#### 8.1.1 Polling

The PLM-1 provides 3 pins which can be used for polling its communication port status (**PDAV** and **PBUSY**) and the communication channel status (**LBUSY**). These pins can be used at all times in SPI mode when **CS** is active. In parallel mode, these signals are available when **CS** is active, **RD** is high and **STRB** is low. These 3 pins are **D0/PDAV**, **D1/LBUSY** and **D2/PBUSY**.

- **PDAV** (Port data available) indicates the PLM-1 has data available for the host to read.

Pin	Name	Serial (0)	Parallel (1)
20	<b>PORTSEL</b>	0	1
10	<b>D0/PDAV</b>	Data Available ( <b>PDAV</b> )	Digital I/O ( <b>D0</b> ) / Data Available ( <b>PDAV</b> )
11	<b>D1/LBUSY</b>	Line Busy ( <b>LBUSY</b> )	Digital I/O ( <b>D1</b> ) / Line Busy ( <b>LBUSY</b> )
12	<b>D2/PBUSY</b>	Port Busy ( <b>PBUSY</b> )	Digital I/O ( <b>D2</b> ) / Port Busy ( <b>PBUSY</b> )
13	<b>D3/MOSI</b>	Serial In ( <b>MOSI</b> )	Digital I/O ( <b>D3</b> )
14	<b>D4/MISO</b>	Serial Out ( <b>MISO</b> )	Digital I/O ( <b>D4</b> )
15	<b>RD/PCKPOL</b>	Serial Clock Polarity ( <b>PCKPOL</b> )	Read/Write selection ( <b>RD</b> )
16	<b>STRB/SCLK</b>	Serial Clock ( <b>SCLK</b> )	Strobe ( <b>STRB</b> )
17	<b>CS</b>	Chip Select ( <b>CS</b> )	Chip Select ( <b>CS</b> )

Table 8-1 PLM-1 host interface pin use in SPI mode and in parallel mode

- **LBUSY** (Line busy) indicates that another transmitter is using the same medium. It is also high when the modem transmits. There is no need for the host to monitor **LBUSY** before transmitting; the transceiver fully implements medium access control logic. **LBUSY** is available to the host for monitoring purposes.
- **PBUSY** (Port busy) indicates the PLM-1 has not finished executing the last read or write operation. This signal must be low before reading or writing data to the PLM-1. This signal is active for up to  $2T_{ref}$  after a read or write operation is completed (where  $T_{ref}$  is the period of  $f_{ref}$ ). Hence, if the host guarantees at least  $2T_{ref}$  between each read or write operation, **PBUSY** does not have to be checked.

## 8.1.2 Parallel port

The parallel mode provides three different operations: polling, reading and writing. A single host can drive multiple modems from a single communication port. **CS** selects which modem is activated for read, write or poll operation. In parallel mode, D0 to D4 are used as data lines, RD determines if the current operation is a read or a write, and the moment of read or write is determined by **STRB** rising edge. Please note that **STRB** may not be shared by several PLM-1s. A typical schematic of the PLM-1 in parallel mode is presented in Figure 8-2.

### 8.1.2.1 Reading

The host reads data according to the following procedure, which is shown on Figure 8-1.

- When idle, always keep the PLM-1 in polling mode (**RD** = 1, **STRB** = 0). The **CS** pin is active low, set by **CSPOL** = 0. Wait for **D2/PBUSY** to be low. Alternatively, if the application guarantees that the last read or write operation was completed at least  $3T_{ref}$  earlier, **PBUSY** is assumed low and need not be polled. The MCU data port pins should be set as inputs.
- Activate **CS**. This pin can also be left always active, when applicable.
- Set **STRB** high. On the **STRB** rising edge, the PLM-1 prepares to load the data on the D port.
- When **HSK** becomes high, valid data is available on the D port. **HSK** always activates within  $2T_{osc}$  after **STRB** is set high.

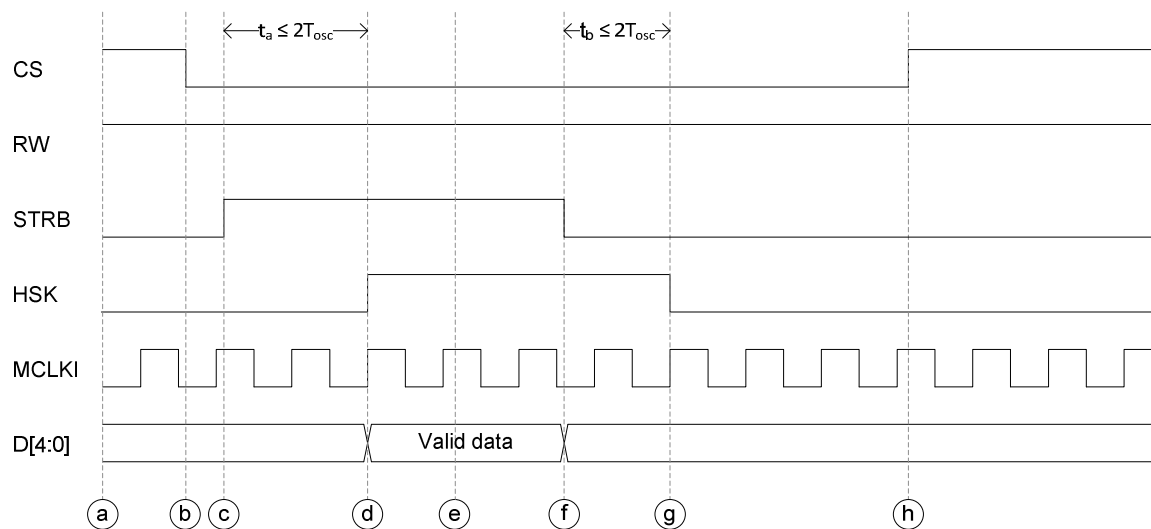


Figure 8-1 Timing diagram of a read operation in parallel mode

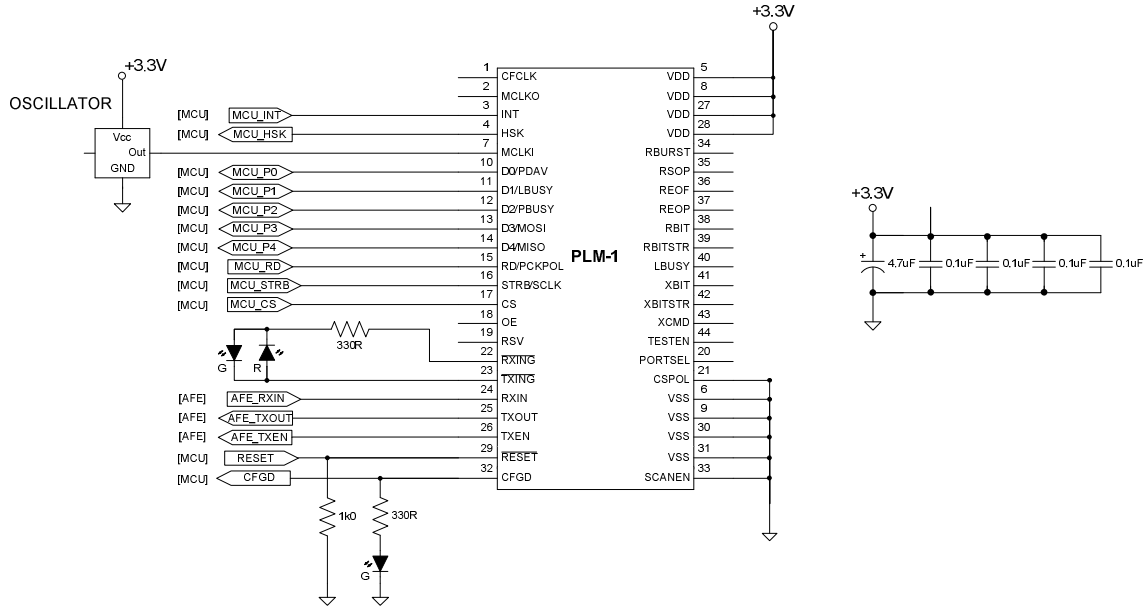


Figure 8-2 Connections of PLM-1 in parallel mode

- e. Read D [4:0] any moment after **HSK** was activated.
- f. Once data is read, set **STRB** to low. PLM-1 output data is considered invalid from this moment.
- g. At most  $2T_{osc}$  after resetting **STRB**, **HSK** goes low.
- h. Deactivate **CS**, according to the polarity defined by **CSPOL**.

Depending on the CPU used, reading and writing is often possible without a waiting period nor **PBUSY/HSK** polling, since the execution time for CPU instructions may guarantee that the minimum prescribed timing is fully respected.

### 8.1.2.2 Writing

The write operation is similar to the read operation. The procedure is described in the following steps (see Figure 8-3):

- a. When idle, always keep the PLM-1 in polling mode (**RD** = 1, **STRB** = 0). The **CS** pin is active low, set by **CSPOL** = 0. Wait for **D2/PBUSY** to be low. Alternatively, if the application guarantees that the last read or write operation was completed at least  $3T_{ref}$  earlier, **PBUSY** is assumed low and need not be polled.
- b. In no particular order, activate the **CS** pin, set the **RD** pin low and output the outgoing data on the D port. Set the MCU data port pins as outputs.
- c. Set **STRB** high. This is the signal that tells the PLM-1 to sample input data D.
- d. Wait for **HSK** to be high then set **STRB** low. Polling **HSK** is optional. **STRB** can be set low as soon as  $2T_{osc}$ , after setting **STRB** high.
- e. Wait for **HSK** to be low or wait  $2T_{osc}$ . The **HSK** falling edge confirms the write operation was performed successfully.
- f. Deactivate **CS** and set **RD** high.

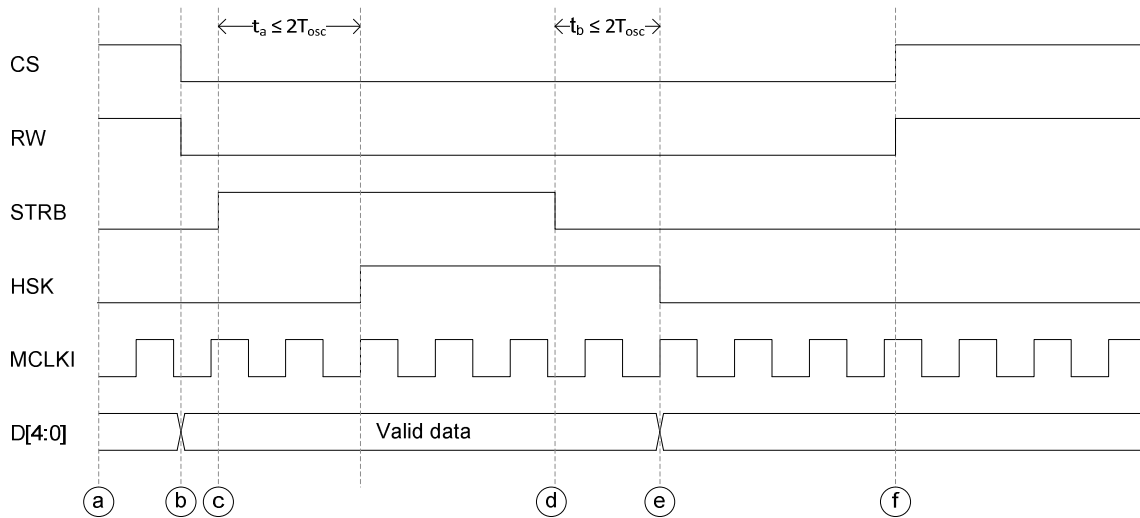


Figure 8-3 Timing diagram of a write operation in parallel mode

### 8.1.3 Serial Peripheral Interface (SPI)

Figure 8-4 shows an example of PLM-1 circuit in SPI mode. In serial mode, the PLM-1 is designed to work as a slave. The serial interface supports SPI clock frequencies up to  $f_{osc}/4$ .

Since SPI transactions are full-duplex, a No Operation code (1Fh) must be written to the PLM-1 while reading a value from it. Alternatively, the PLM-1 outputs a No Operation code (1Fh) when performing a read + write operation while no data needs to be read.

The **PCKPOL** pin determines the polarity of the clock when the data is received and transmitted on the SPI bus. If **PCKPOL** is high, the output data (**MISO**) is generated on the rising edge and the input data

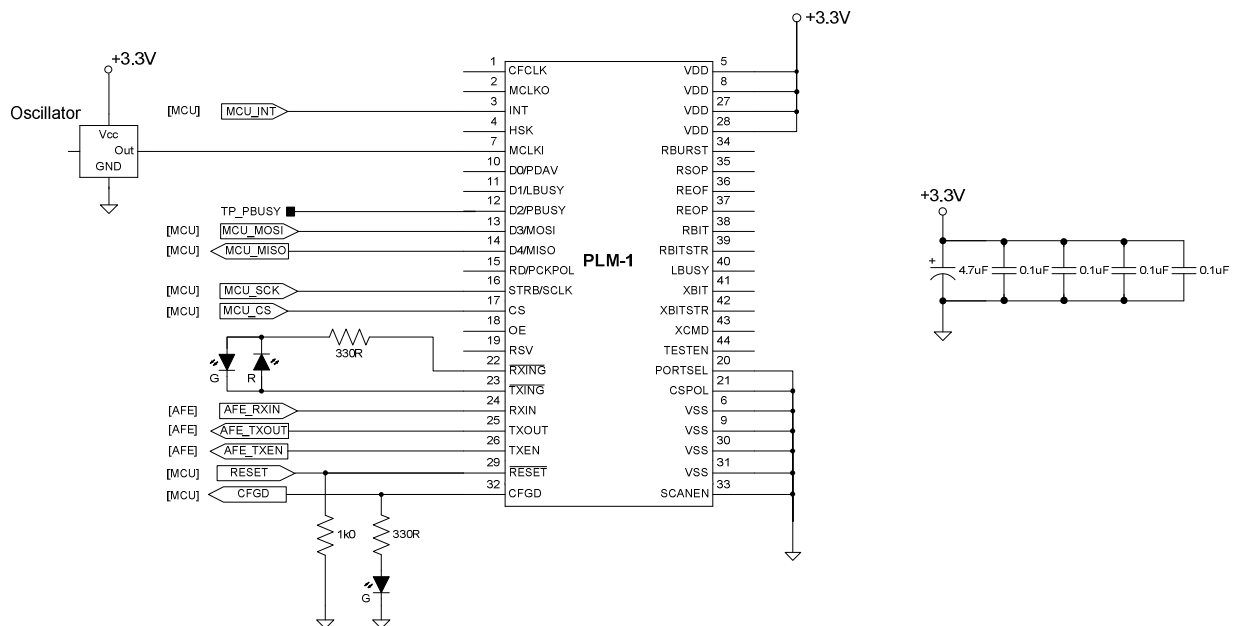


Figure 8-4 Connections of PLM-1 in SPI mode

(**MOSI**) is sampled on the falling edge of the SPI clock (pin **SCLK**), which is low in idle state.

Alternatively, if **PCKPOL** is low, the idle state of the **SCLK** must be high. In this case, the PLM-1 generates its output data on the falling edge of the SPI clock and it samples the input data on its rising edge. Table 8-2 explains how the host should assert port pins to read and write the data based on the polarity of **PCKPOL** pin.

All SPI transfers are 8-bits, with the Most Significant Bit transmitted first. The PLM-1 uses only bits 0 to 4 and ignores bits 5 to 7. For future compatibility, the ignored bits must always be zero.

The timing diagram shown in Figure 8-5 illustrates the steps to follow when sending a nibble to the PLM-1 using the SPI interface. The hardware configuration used in this case is **PCKPOL** = 1 (clock idle state = low, data setup on rising edge, data sampling on falling edge) and **CSPOL** = 0 (Chip Select active low). This configuration is recommended.

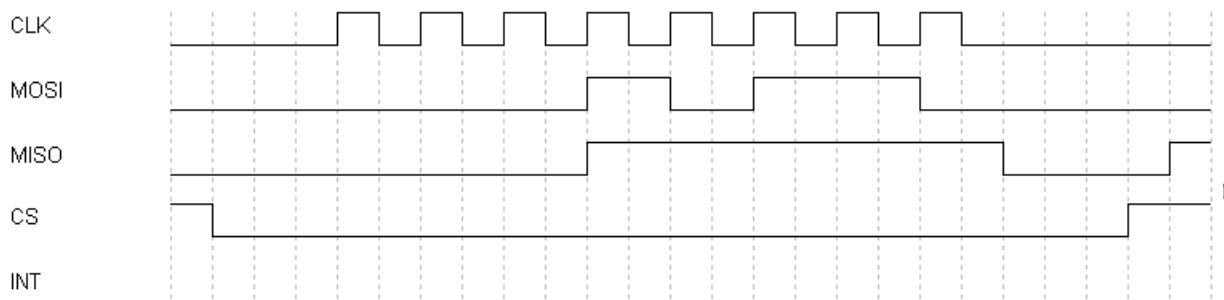
In this example, the host is sending a **SOFT\_RESET** command (16h), while reading a **NOP** code (1Fh) from the PLM-1.

Although these settings of **PCKPOL** and **CSPOL** should be used by default, it is convenient in some applications to make the PLM-1 **CS** polarity active high or to change the SPI configuration of the chip. This can be done by modifying the pins **CSPOL** and **PCKPOL**. The following timing diagram shows the reception of a data nibble on a system in which **PCKPOL** = 0 and **CSPOL** = 1.

In Figure 8-6, the interrupt line (high) indicates the PLM-1 has information to write to the host. The interrupt goes low on the first clock transition. When reading data, the host has to send a **NOP** code (1Fh) to the PLM-1, which is present on the **MISO** line. In **MISO**, the data nibble 0Ah is read by the host. It is also important to note that by setting **PCKPOL** = 0, the host must provide an SPI clock with a high idle state. It also has to set its data on the falling edge of the clock, and sample data on the rising edge.

<b>PCKPOL</b>	<b>Clock Idle State</b>	<b>Edge for Data Setup</b>	<b>Edge for Data Sampling</b>
High	Low	Rising edge	Falling edge
Low	High	Falling edge	Rising edge

**Table 8-2 PLM-1 SPI configuration depending on the PCKPOL pin**



**Figure 8-5 A SOFT RESET written to the PLM-1 through the SPI interface (PCKPOL = 1, CSPOL = 0)**

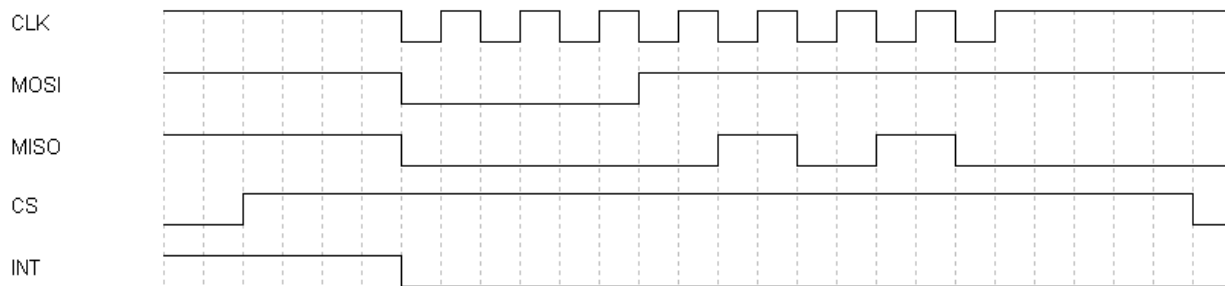


Figure 8-6 Data received (0x0A) by the PLM-1, transferred to the host (PCKPOL = 0, CSPOL = 1)

## 8.2 Configuration Procedure

The C code shown in Figure 8-7 presents a way of configuring the PLM-1. The function argument is the 38-nibble configuration string stored in a 19-byte array. First a SOFT\_RESET command is written to the PLM-1, and then the 38 configuration nibbles follow. In the end, the **CFGD** pin is read to make sure the PLM-1 was correctly configured. The External interrupt of the host should be disabled during this procedure and re-enabled after configuration.

Although PLM-1 firmware libraries provided by Ariane Controls automatically computes configuration strings, advanced users can use the ACES software to specify new communication parameters and obtain configuration strings adapted to their needs. Still, using the firmware libraries with data from Table A-1 in Appendix A yields optimized results.

```
int plm1_configure( uint8_t *cfg_string )
{
    int i = 19;

    /* Sends a Soft reset command to the PLM-1. */
    exchange_nibble( 0x16 );

    /* Sends the nibble sequence to the PLM-1. */
    do
    {
        exchange_nibble(*cfg_string >> 4 );
        exchange_nibble(*cfg_string++ & 0x0F );
    } while( --i > 0 );

    /* Verify pin CFGD of PLM-1. */
    if( read_pin(PLM_CFGD_PIN) == 1 )
        return 1;
    else
        return 0;
}
```

Figure 8-7 Pseudo-code for configuring the PLM-1

## 8.3 Transmitting and Receiving

Once the PLM-1 is configured, the host is able to transmit and receive packets. This section describes the procedure to follow in order to transmit packets successfully.

PLM-1 offers half-duplex communication, which implies rules to coordinate transmissions and receptions. The state machine in Figure 8-8 presents five different states that should be handled by the host. These states are: Configuring, Idle, Negotiating, Transmitting and Receiving.

### 8.3.1 Configuring

Before anything else, the PLM-1 must be configured. Once it is configured, it goes in idle state.

### 8.3.2 Idle

In idle state, the PLM-1 is monitoring the channel, detecting preamble bursts and packets. This is the default state. The idle state is reached:

- After configuration.
- After a packet is received successfully
- After a packet reception is aborted
- After a packet is transmitted successfully
- After a packet transmission is aborted

### 8.3.3 Negotiating

From idle state, the PLM-1 goes in negotiation state when the host writes a single data nibble to the PLM-1 through the communication port. This first nibble of the packet determines the packet priority. The preamble is being transmitted during this state.

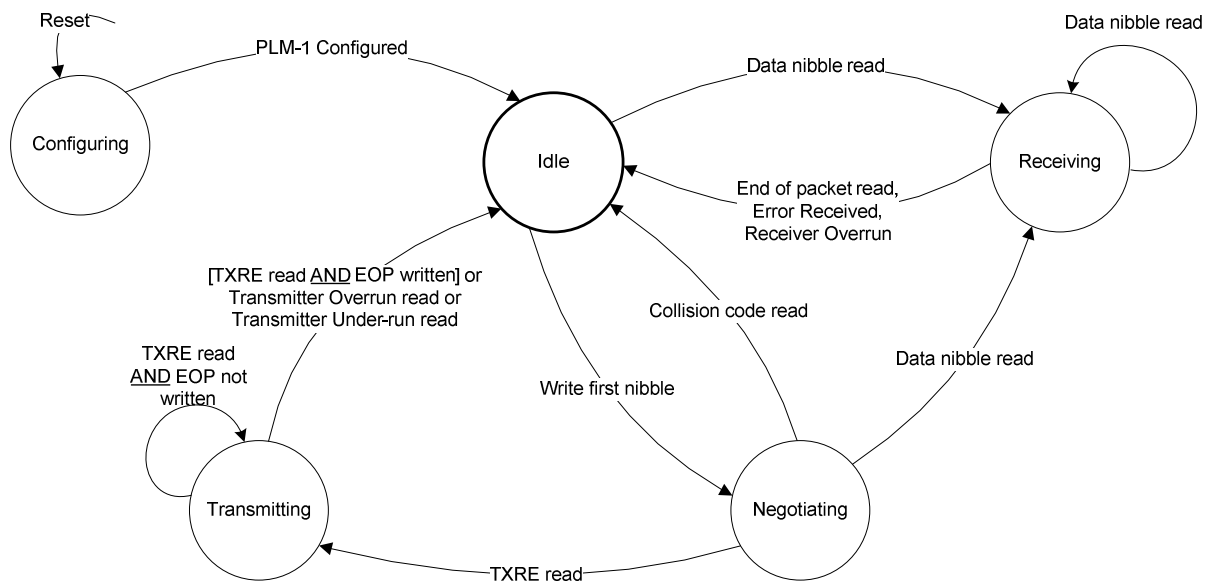


Figure 8-8 PLM-1 Operation as a Finite State Machine

If a PLM-1 in negotiation state detects a preamble from another node, it releases a COLL (collision) code to the host. In this case, the host returns in idle state, ready to restart transmission or start receiving. If a data nibble is received during the preamble, the host enters the receiving state immediately. Finally, if the preamble gets transmitted completely without detecting any collision, an interrupt with a TXRE code is generated and host enters Transmitting state.

In case configuration parameter NOPREAM is 1, there is no collision, but it is still possible that a data nibble is being received while the host is writing the first nibble to the PLM-1.

### 8.3.4 Transmitting

The only way to enter Transmitting state is by reading control code TXRE after an interrupt. This also marks the end of the negotiating state. In this case, the next nibble to transmit must be written to the PLM-1. Afterwards, the PLM-1 will trigger another interrupt with TXRE code requesting for the next packet nibble. This cycle goes on until the entire data packet has been transferred. When the EOP code is written to end the packet, the host remains in transmitting state until the last TXRE is read from the PLM-1, after which it goes back in idle state.

Idle state is also reached after Transmitter Overrun and Transmitter Under-run errors. In these cases, transmission may be restarted immediately.

### 8.3.5 Receiving

The host enters Receiving state as soon as it reads a data nibble from the PLM-1. It remains in this state as long as data nibbles keep being received. It goes back to idle state when an EOP is received, or when an error in reception or a receiver overrun occur.

## 9 Analog Front-End

The Analog Front-End (AFE) is the interface between the PLM-1 modem and the communication channel. This circuit (Figure 9-1) performs several signal conditioning operations: sine-square conversion, filtering, amplification and coupling. It is composed of three main sections: receiving circuit (Rx), transmitting circuit (Tx) and coupling circuit. As the two circuits operate independently, bidirectional transceivers (Tx-Rx) or receive-only devices (Rx) can be designed.

### 9.1 AFE Operation

#### 9.1.1 Rx Circuit

In receiving mode, the communication signal is processed by the Rx filter that eliminates the out-of-band frequencies. Then, the sinusoidal signal is converted to a 3.3V square wave that is applied to the modem **RXIN** pin.

A narrowband band-pass filter centered on the communication frequency ( $f_c$ ) is usually recommended to remove the background noise. Also, the Rx filter blocks communication signals at different frequencies, allowing a transceiver to share the powerline medium with other systems and technologies.

The Rx filter output can be amplified by a fixed or variable gain in order to improve the signal-to-noise ratio.

An integrated voltage comparator is typically used to create the digital signal required at the modem input (**RXIN**). The converter's ability to detect very low signals can enhance the receiver sensitivity, thus improving the communication performance in extremely loaded and noisy environments.

#### 9.1.2 Tx Circuit

The PLM-1 transmit signal (**TXOUT**) is filtered, amplified, then coupled on the communication channel.

The Tx filter converts the PLM-1 square-wave output into a sinusoidal signal and attenuates the  $f_{ref}$  frequency component, the two auxiliary frequencies and all related harmonics. Narrowband band-pass filters or low pass filters with steep attenuation slope near the cut-off frequency are typically required. An attenuation of minimum 15dB between the center frequency and  $f_{ref}$  is recommended. Constant gain within the passband (low ripple) is also desirable.

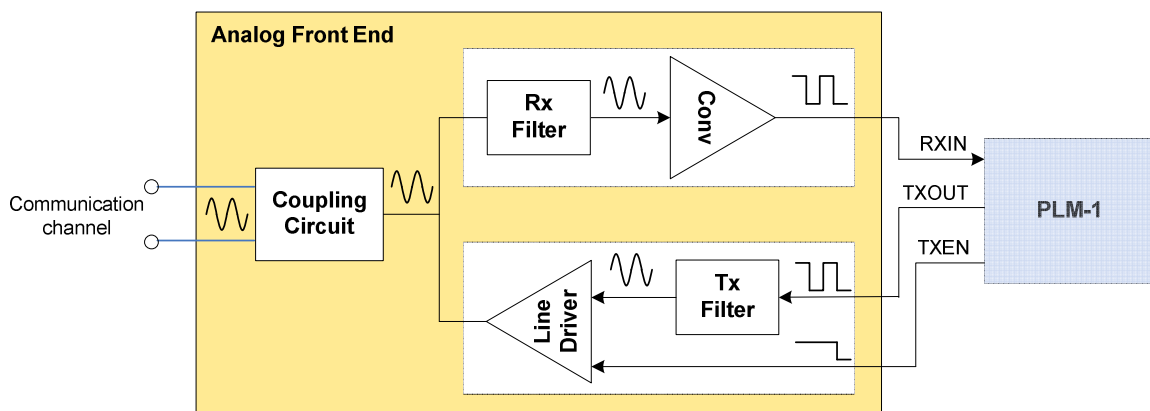


Figure 9-1 Block diagram of Analog Front-End

The line driver provides voltage and current signal amplification. The amplifier design and its power requirements depend on the application conditions, particularly the impedance of the communication channel. High power amplifiers are typically required to drive low impedance power lines.

The PLM-1 provides an enable signal (**TXEN**) activated during the transmission of a packet. This signal is used to enable the line driver during the transmission and switching it off when in idle or receiving mode. This allows reducing the power consumption and avoiding the low output impedance of the Tx circuit attenuating the communication signals on the line.

### 9.1.3 Coupling Circuit

The coupling circuit performs the connection with the communication channel. It acts as a filter that passes the communication signals, while attenuating out-of-band frequencies. Its design mainly depends on the line characteristics, such as voltage, frequency, wiring style, etc. In some applications, the coupling circuit can be required to provide safety isolation and protection from high voltage disturbances.

## 9.2 Filter Design

External filtering is a key feature of PLM-1-based transceivers, which allows operation in a wide range of communication frequencies. The filters design is related to the application conditions, particularly the power line noise for the Rx filter and the conducted emissions constraint for the Tx filter.

### 9.2.1 Filter Characteristics

The basic requirements for the filter design are described below.

#### 9.2.1.1 Frequency Response

Narrowband band-pass response centered at the communication center frequency ( $f_c$ ) is typically recommended (Figure 9-2a).

Low-pass response with high quality factor (Q) can also be considered (Figure 9-2b). The peak in the low-pass response should be centered on the communication center frequency  $f_c$ .

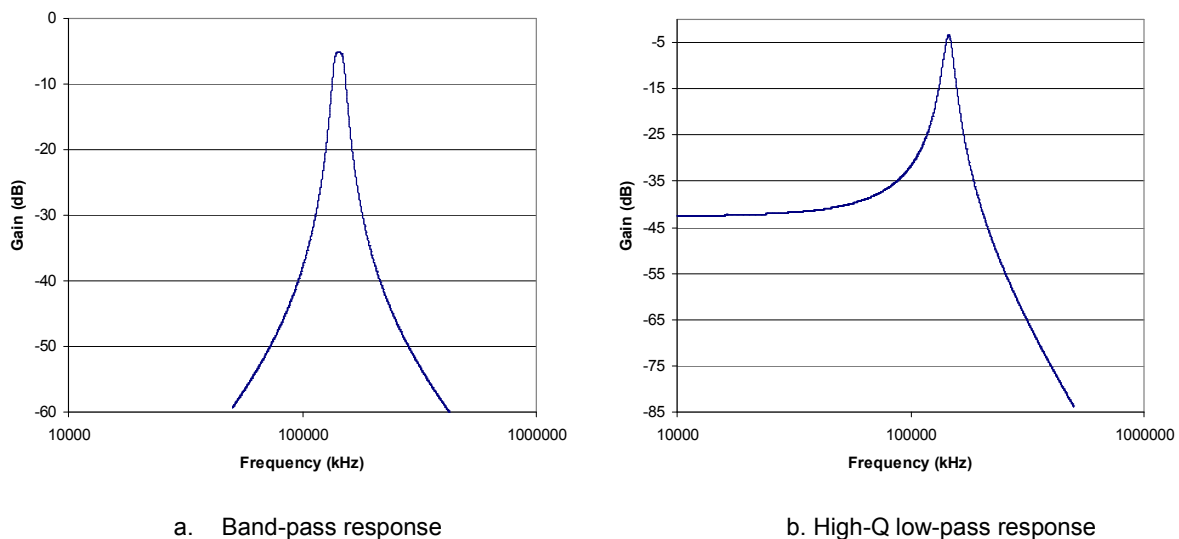


Figure 9-2 Typical frequency response of Tx and Rx filters

**9.2.1.2 Bandwidth**

The filter passband should be wide enough to accommodate the two communication frequencies  $f_0$  and  $f_1$  at the intended configuration, and narrow enough to selectively attenuate out-of-band signals. Typically, the -3dB bandwidth should be equal or slightly greater than the maximum intended data rate.

The filter may have a positive or negative gain (dB) in the passband, i.e. it can amplify or attenuate the bandpass signal. However, passband attenuation should be limited (up to 8-10dB), since too much insertion loss would require high signal amplification in subsequent stages.

Adding a positive gain to the filtered signal in reception can improve the receiver sensitivity. However, increasing the gain could also amplify unwanted noise in the passband.

**9.2.1.3 Roll-off and Stopband Attenuation**

A sharp slope characteristic is desirable near the cut-off frequencies in order to "isolate" the communication signals from out-of-band signals and noise. This slope may not continue in the stopband. Actually, the stopband attenuation is mainly related to the accepted level of harmonic frequencies in the transmitted signal.

For the Rx filter, an attenuation of at least 15dB at  $f_c \pm 20\text{kHz}$  is recommended. Usually, a two-stage 4<sup>th</sup>-order filter is necessary to attain this roll-off characteristic.

In the case of the Tx filter, the roll-off and stopband attenuation depend on the applicable regulations regarding the limits of conducted emissions:

- The US FCC Part 15 [1] and Canada’s ICES006 [2] limit the harmonics and unwanted emissions falling within 535kHz-1705kHz at 1000µV (60dBuV) measured at the transceiver output across a 50Ω line impedance stabilization network (LISN).

This can be accomplished by choosing the communication frequency below 175kHz and using a 4<sup>th</sup>-order filter in transmission, which should provide more than 15dB of attenuation at  $f_c \pm 20\text{kHz}$  and 60dB of attenuation above 535kHz.

- The European CENELEC EN 50065-1 [3] provides the following limits for the conducted emissions:

Frequency Range	Out-of-band signals (dBuV)
3kHz to 9kHz	Below 89dBuV (peak)
9kHz to 500kHz	Decreasing linearly with the logarithm of frequency from 89 to 56dBuV (quasi-peak)
500kHz to 5MHz	Below 56dBuV (quasi-peak)
5MHz to 30MHz	Below 60dBuV (quasi-peak)

As the CENELEC requirements are more severe, a highly selective Tx filter with steeper response needs to be designed. An 8<sup>th</sup>-order filter should be considered for providing a minimum attenuation of 30dB at  $f_c + 20\text{kHz}$  and 54dB at  $f_c + 40\text{kHz}$ . An attenuation of 68dB in the stopband (above 500kHz) is adequate.

To meet the above requirements, a low-pass response with high quality factor ( $Q \geq 10$ ) is recommended, as it can provide steeper roll-off than a standard band-pass filter of the same order (Figure 9-2).

If conducted emissions regulations don’t apply, a 4<sup>th</sup>-order filter with an attenuation of at least 15dB at  $f_c \pm 20\text{kHz}$  can be used in transmission.

## 9.2.2 Filter Examples

Various types of filters can be considered to implement the above requirements: passive circuits, active circuits or ceramic devices.

### 9.2.2.1 Passive Filters

The passive filters use the opposite frequency-selective properties of the inductors and capacitors. They work well at low and high frequencies and generate little noise when compared with circuits using active elements. Also, the passive filters require a low number of components for the implementation of a given transfer function.

On the other hand, they cannot provide positive signal gain. Also, there are limitations and constraints regarding the selection of inductors if high accuracy (1% or 2%, for example), small size, or large values are required. Capacitors are rather used for tuning the filter characteristics, e.g. by connecting several capacitors in parallel.

Figure 9-3 shows a two-stage 4<sup>th</sup>-order band-pass filter that can be used for both Rx and Tx circuits. It is centered at 144kHz, has a bandwidth of about 15kHz at -3dB, less than 8dB of insertion loss, and provides about 15dB of attenuation at  $f_c \pm 20$ kHz (frequency response shown in Figure 9-2a). With more than 60dB of attenuation at 535kHz, this filter allows compliance with FCC part 15 requirements for conducted emissions when used in transmission.

A tolerance of 5% or better is recommended for capacitors and inductors. Also, the inductors should have high quality factor ( $Q > 10$  at  $f_c$ ) and self-resonant frequency as far as possible from the operating frequency.

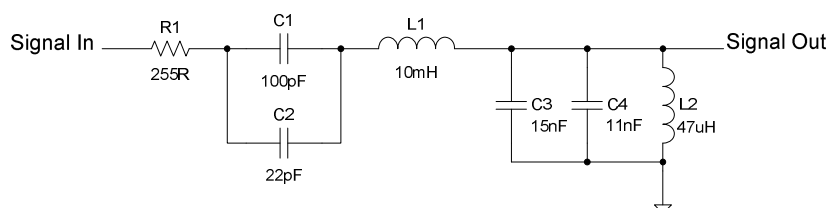


Figure 9-3 Fourth-order 144kHz band-pass passive filter for Tx and Rx

### 9.2.2.2 Active Filters

Active filters combine active circuit devices (operational amplifiers) with resistors and capacitors. They allow designing superior filtering characteristics, provided that low tolerance resistors and capacitors are used. Also, active filters allow easier adjustment of the frequency response, being of particular interest when different communication frequencies need to be tested.

However, active filters are typically more expensive and require a power supply. Also, the performance at high frequencies is limited by the gain-bandwidth product of the amplifying elements.

Figure 9-4 presents a two-stage 4<sup>th</sup>-order low-pass filter topology that provides a frequency response as in Figure 9-2b. The high quality factor ( $Q=10$ ) creates a peak in the amplitude response, which acts as a band-pass characteristic centered at 144kHz. The filter provides a bandwidth of about 10kHz at -3dB, less than 3dB of insertion loss, about 18dB of attenuation at  $f_c + 20$ kHz and more than 75dB at 535kHz. This filter can be used in transmission for compliance with FCC part 15, as well as in reception.

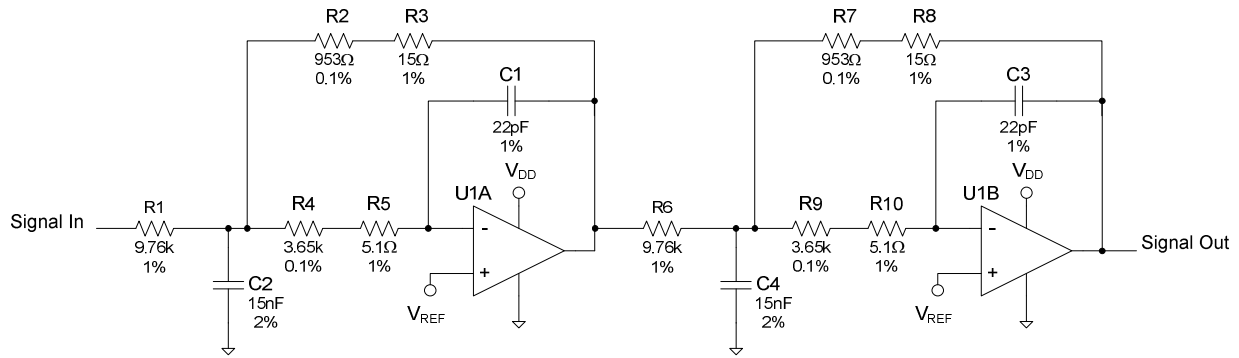


Figure 9-4 Fourth-order 144kHz high-Q low-pass active filter for Tx and Rx

Figure 9-5 shows an alternate active filter for the Rx circuit, intended to improve the receiver sensitivity by adding a gain of 4 in the passband. The filter response is centered at 144kHz, has a bandwidth of about 11kHz at -3dB, and provides about 16dB of attenuation at  $f_c + 20$ kHz.

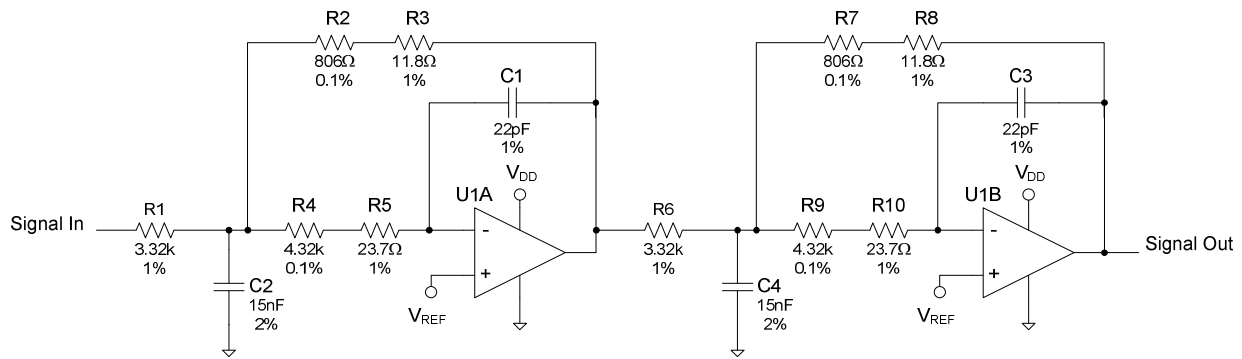


Figure 9-5 Fourth-order 144kHz high-Q low-pass active filter for Rx

When the compliance with CENELEC requirements for conducted emissions is mandatory, a more selective frequency response is required. Figure 9-6 shows an 8<sup>th</sup>-order low-pass active filter with high quality factor ( $Q=8$ ), centered at 144kHz. The filter provides a bandwidth of about 8kHz at -3dB, about 32dB of attenuation at  $f_c + 20$ kHz and more than 56dB at  $f_c + 40$ kHz.

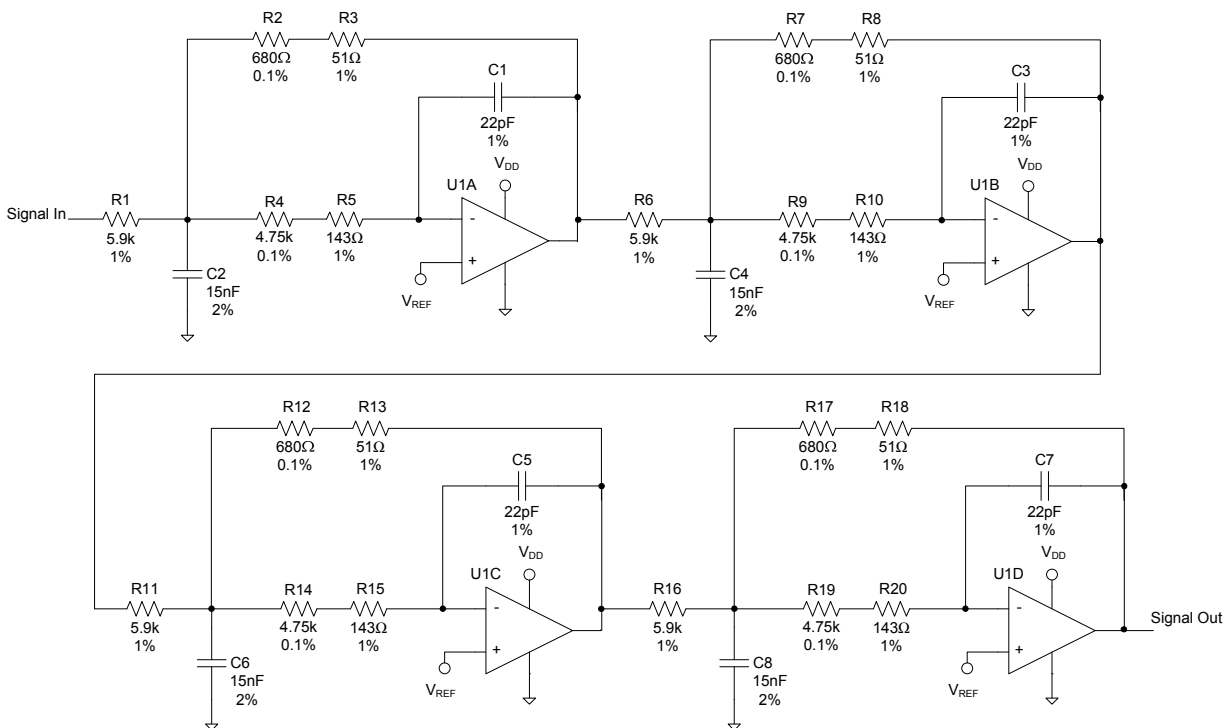


Figure 9-6 Eight-order 144kHz high-Q low-pass active filter for Tx

### 9.2.2.2.1 Component Selection

The component selection is very important when designing or using this type of filter. The operational amplifier must be fast enough to avoid problems with non-linear distortion and filter response distortion. The most important parameter is the Gain Bandwidth Product (GBWP) of the operational amplifier. In general, the open-loop gain should be 100 times (40 dB above) the peak gain of a filter section to allow a maximum gain error of 1% [4]. A rough estimate of the minimum GBWP required for the op amp is:

$$GBWP = 100 \times \sqrt[n]{G} \times f_c,$$

where  $G$  is the filter gain,  $f_c$  is the center frequency, and  $n$  is the filter order, i.e. the number of  $2^{nd}$ -order stages connected in series.

Besides good DC performance, low noise and low signal distortion, another important parameter that determines the speed of an op amp and its ability to handle large signals is the slew rate (SR). For adequate full-power response, the minimum slew rate should be:

$$SR = \pi \times V_{out_{pp}} \times f_c.$$

Table 9-1 provides a selection of recommended operational amplifiers and their characteristics (at 5V single-supply voltage).

Part number	Manufacturer	GBWP (MHz)	SR (V/us)	THD (dB)
FHP3130, FHP3230, FHP3430	Fairchild Semiconductor	60	105	55
TSH7x, TSH8x,	STMicroelectronics	65	104	61
LT1813, LT1814	Linear Technology	94	350	75
OPA2354, OPA4354	Texas Instruments	100	150	75

**Table 9-1 Examples of operational amplifiers for active filters**

For single-supply op amps, the potential of the non-inverting input should be level-shifted to midrail. A resistive voltage divider circuit can be used to generate  $V_{REF}$  from the supply voltage ( $V_{DD}$ ).

The tolerance of the capacitors and resistors has an impact on the filter performance and stability. Both center frequency and quality factor are affected by changes in component values. Particularly in the case of higher-order filters, small differences in  $Q$  and  $f_c$  values in each stage can significantly modify the overall filter response from its intended characteristic.

NP0 (C0G) ceramic capacitors are recommended, as they are more stable over temperature and voltage. A tolerance of 1% or 2% should be used.

For best results, 0.1% resistors are recommended, since they are commonly available and relatively cheap for a wide range of values. For better precision, the resistance values can be set using two resistors in series. The resistor values should stay below 100k $\Omega$  to avoid excessive resistor noise.

#### 9.2.2.2 Ariane Active Filter Designer

The Ariane Active Filter Designer is a software tool that helps designing and analyzing high-Q low-pass active filters for use with the PLM-1 modem in transmission and reception.

Below is a list of the main features provided by the software:

- Design new filter from desired characteristics
- Analyze the frequency response of existing filter design
- Save filter design for future analysis or modification
- Display amplitude and phase response with customizable cursors for analysis
- Show the filter response deviation caused by the component tolerance
- Provide filter schematic with component values

The software is available for free download at [www.arianecontrols.com](http://www.arianecontrols.com)

#### 9.2.2.3 Ceramic Filters

The ceramic filters are made of piezoelectric ceramics used as mechanical resonators. These inexpensive devices have precisely defined center frequency, narrow passband and very good selectivity near the cutoff frequencies. However, they usually provide limited attenuation in the stopband and exhibit spurious response at some frequencies. Also, their response can be affected by mechanical vibration or shocks.

Part number	Manufacturer	F <sub>c</sub> (kHz)	6dB Bandwidth (kHz)	Stopband Attenuation (dB)	Insertion loss (dB)	Input/Output Impedance (k $\Omega$ )
FM262AL	Ariane Controls	262 $\pm 1$ kHz	5.0 min	20 at F <sub>c</sub> $\pm 100$ kHz	5.0 max	1.0 / 1.5
CFWKA450KGFA-R0	Murata	450 $\pm 1.5$ kHz	9.0 min	50 at F <sub>c</sub> $\pm 100$ kHz	6.0 max	1.5 / 1.5
CFUKG455KF4X-R0	Murata	455 $\pm 1.5$ kHz	12.0 min	27 at F <sub>c</sub> $\pm 100$ kHz	6.0 max	1.5 / 1.5
CFUKF455KD1X-R0	Murata	455 $\pm 1.0$ kHz	20.0 min	23 at F <sub>c</sub> $\pm 100$ kHz	7.0 max	1.5 / 1.5
CFUKF455KB4X-R0	Murata	455 $\pm 1.5$ kHz	30.0 min	25 at F <sub>c</sub> $\pm 100$ kHz	5.0 max	1.0 / 1.0

Table 9-2 Examples of ceramic filters

These devices can be considered as Rx filters for low-cost receivers. They can also be used in transmission in applications where requirements for conducted emissions are not mandatory (e.g., communication on DC line or un-powered line).

Band-pass ceramic filters centered at 450kHz or 455kHz are commercially available from a few manufacturers (Murata, for example). Custom-made ceramic filters at 262kHz are also available from Ariane Controls (FM262AL). Table 9-2 provides a few examples of ceramic filters and their characteristics.

## 9.3 Line Driver Design

The line driver provides voltage and current signal amplification in transmission, in order to keep the signal transmitted on the line as high as possible, thus ensuring reliable communication at long distance.

While a power amplifier is always required to transmit the PLM-1 signals on a line, its design depends on the application requirements. Several criteria should be considered when selecting or designing the amplifier, including the typical line impedance, network topology and maximum length, tolerable signal distortion, available DC power, etc.

### 9.3.1 Line Driver Characteristics

Below are described the main parameters to be considered when selecting or designing a line driver.

#### 9.3.1.1 Bandwidth

The amplifier must operate properly in the range of communication frequency, i.e. provide a constant gain and sufficient power.

There are several parameters related to the frequency response of operational amplifiers, like unity-gain bandwidth, gain-bandwidth product or full power bandwidth. The variation of the maximum output signal versus frequency is also a useful indication of the op amp performance at the intended communication frequency.

### 9.3.1.2 Maximum Output Voltage Swing

The amplifier should be able to provide at the output the required voltage amplitude, without waveform clipping.

The maximum transmitter output voltage can be limited by the applicable regulations. For example, CENELEC EN 50065-1 [3] limits the transmission level for single-phase general use devices (Class 122) at 122dBuV (3.5Vp-p); Class 134 equipment (that may require prior notification) can transmit up to 134dBuV (14Vp-p). These voltages are measured using artificial networks conforming to CISPR 16-1:1993. Industry Canada ICES006 [2] limits the permissible output voltages for installation in residential and office buildings at 15Vp-p, measured across a 50Ω load. The limit of 15Vp-p usually applies to residential and commercial devices in US.

### 9.3.1.3 Maximum Output Current

The amplifier capability to drive high output current is directly related to the line impedance at the communication frequency. Lower the line impedance, higher the amount of current that is drawn from the amplifier output.

The impedance of low-voltage indoor power line is highly dependent on the network topology and connected loads, and typically ranges between a few Ohms and several hundred Ohms. Extremely low values can be caused by capacitive loads connected in close proximity of the transceiver (e.g., home appliances with integrated EMI filters). Even lower impedance values can be found in outdoor low-voltage distribution systems, mainly because of the large capacitors used for power factor correction. The DC micro-grids transporting energy from solar panels and other alternative sources may also have low impedance caused by the filter capacitors associated with DC/AC inverters.

For applications where the line impedance can be as low as a few Ohms, high current amplifiers are required, in order to maintain the level of transmitted signal as high as possible. An output current of 1A or more is typically recommended.

### 9.3.1.4 Thermal Protection

The power amplifier temperature may considerably increase when transmitting continuously in very low impedance conditions. To avoid overheating, adequate heat sink area and thermal shutdown capability should be considered for the line driver.

### 9.3.1.5 Harmonic Distortion

In applications where requirements for conducted emissions apply, the line driver must be able to provide low harmonic distortion of the output signal (typically at least 60dB at the communication frequency).

### 9.3.1.6 Output Disable Control

PLM-1's enable signal (TXEN) can be used to control the activation of the line driver only during transmission. The amplifier disable capability allows reducing the power consumption in idle mode and preventing the low output impedance of the Tx circuit attenuating the communication signals on the line.

## 9.3.2 Line Driver Options

Depending on the application requirements, various types of amplifiers can be used as line driver. There are two categories to consider when designing the power amplifier: discrete or integrated circuits.

### 9.3.2.1 Discrete Power Amplifier

Discrete analog amplifiers can be an option when high power is required, since external transistors allow for better heat dissipation. Also, while these circuits generally require more parts than integrated amplifiers, typical designs are still cost-effective.

Several types of analog power amplifiers can be used for the design of the PLM-1 line driver, like class A, B, AB and C circuits.

Class A amplifiers are typically more linear and less complex than other types, but are very inefficient and can require significant heat dissipation. This type of amplifier can be used as line driver only for low-power requirements (such as communication on un-powered lines). Also, class A designs can be used as low-power signal amplifier in reception.

Class C design can provide high efficiency, but also potentially high output distortion. However, used as line driver with PLM-1, the distortion can be considerably reduced with a tuned output LC filter.

Class B and AB push-pull circuits are the most common design types. Class B amplifier has much better efficiency than class A, but suffers from signal crossover distortion caused by the transition between the operation of the two complementary output transistors. A line driver based on class B design can be a good option if signal harmonics are allowed. Class AB amplifier allows greatly minimizing or eliminating the crossover distortion by using a slight forward bias in the base circuit such that the push-pull transistors are idling at a small output current. While class AB sacrifices some efficiency over class B in favour of linearity, it can be considered as a good compromise for transceiver line driver when low signal disturbance is required.

Figure 9-7 shows an example of class B design that allows delivering high current into low impedance lines. A class AB design with slightly lower output current, but better linearity is shown in Figure 9-8. In both examples, an operational amplifier is used to provide easy adjustable voltage gain. The feedback resistor  $R_f$  allows setting the level of transmitted signal, according to the application requirements and available supply voltage ( $V_{DD}$ ). The maximum output current can be adjusted with output resistors R8 and R9. The PLM-1 enable signal (**TXEN**) is used to activate the amplifier only during transmission. This allows reducing the power consumption and avoiding the low output impedance of the Tx circuit attenuating the communication signals on the line. In the class AB design, the output stage is also switched off when not transmitting, because of the quiescent current through the output transistors.

An important design consideration is related to the output current and temperature dissipation. The amplifier output current may considerably increase when transmitting in very low impedance. Push-pull transistors Q1, Q2, as well as output resistors R8, R9 must be rated for the maximum power. Also, to avoid overheating during long transmissions, bipolar transistors Q1 and Q2 must be provided with thermal connection to an adequate heat sink area.

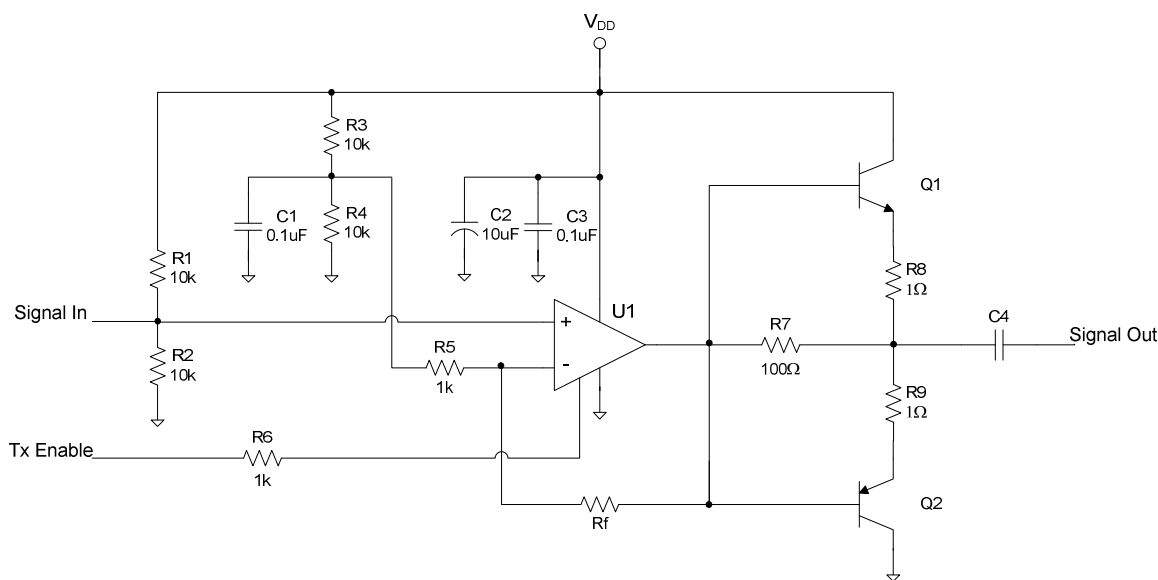


Figure 9-7 Class B power amplifier

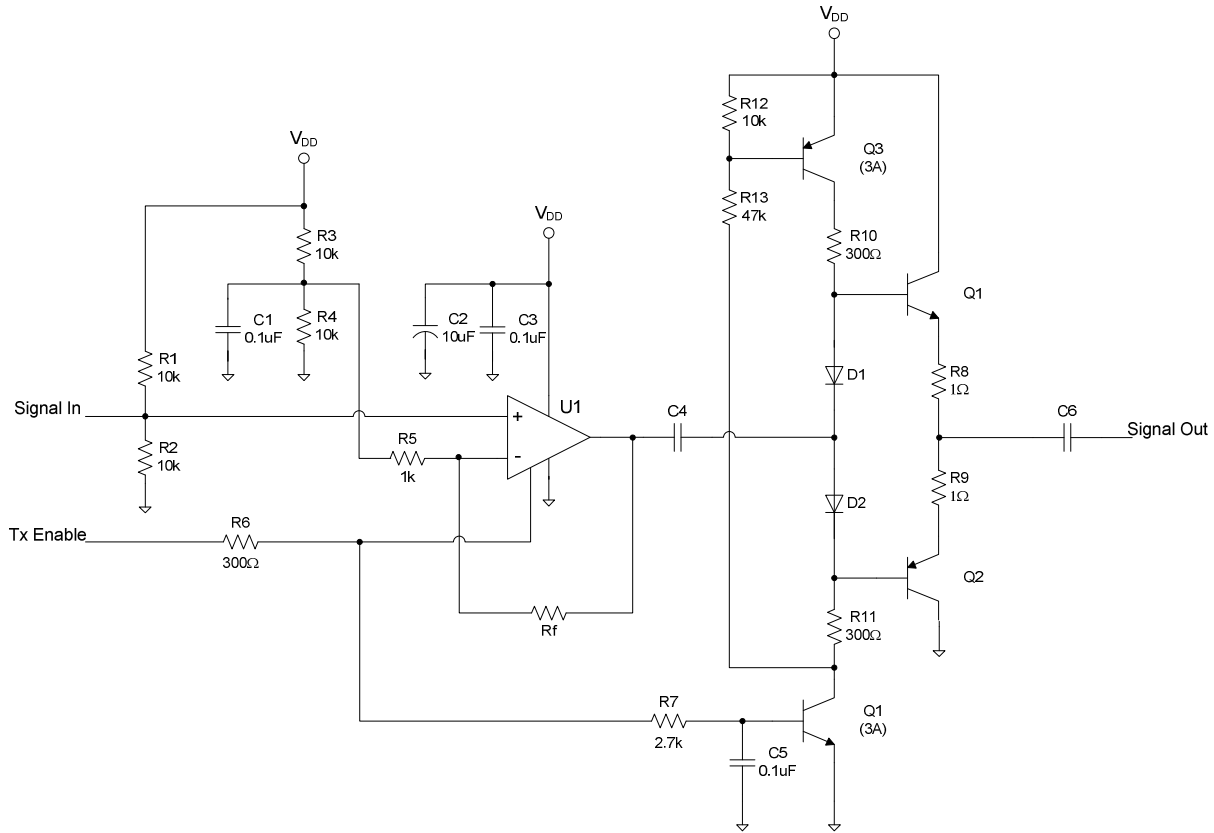


Figure 9-8 Class AB power amplifier

9.3.2.2 Integrated Power Amplifier

Using an integrated power amplifier as line driver has some advantages, such as small footprint on PCB, low part count and easy design. While there is a large selection of power amplifiers available, there are only a few models specifically intended for power line transceivers. Table 9-3 presents a few examples, with different output power capabilities.

Part number	Manufacturer	Gain Bandwidth Product	Max Vout	Max Iout	THD + Noise	Output Disable	Thermal shutdown
OPA561	Texas Instruments	17MHz	12Vp-p	1.2A	-74dB	Yes	Yes
OPA564	Texas Instruments	17MHz	20Vp-p	1.5A	-90dB	Yes	Yes
NCS5650	On Semiconductor	60MHz	10Vp-p	1.5A	-76dB	Yes	Yes
ACPL-0820	Avago	3MHz	7Vp-p	0.75A	~ -70dB	Yes	Yes

Table 9-3 Examples of integrated line drivers

## 9.4 Coupling Circuit Design

The coupling circuit connects the AFE to the communication channel. It is typically made of passive components (capacitors, inductors, transformers) that are arranged in filter topology to efficiently pass the communication signals, while attenuating out-of-band frequencies.

### 9.4.1 Coupling Circuit Characteristics

The design of this circuit is highly dependent on the line characteristics, such as voltage/current amplitude and frequency, disturbances, wiring style, location, applicable regulations, etc. Below are described the main parameters that should be considered when designing the coupling circuit.

#### 9.4.1.1 Low Signal Loss

A key requirement of any coupling circuit is to maintain a low impedance path for the communication signal so that the signal loss is minimized. This can be achieved by designing the coupling circuit to act as a filter that passes the communication signal with minimum attenuation.

#### 9.4.1.2 Isolation

In some applications, the coupling circuit can be required to provide safety isolation between the AFE and communication line, for example to avoid that the mains Neutral wire is connected directly to the circuit board ground.

The galvanic isolation is usually achieved with a transformer. In addition to provide the required isolation level, this transformer must have appropriate characteristics to pass the high-frequency communication signals with minimal loss and distortion: low DC resistance, low winding capacitance, low leakage inductance, high magnetizing inductance, and high saturation level.

#### 9.4.1.3 Surge Protection

Coupling circuits that connect to AC or DC power lines must also provide protection from high-voltage disturbances. The required level of surge protection generally depends on the power line environment and the location where the product is installed. For example, the surge levels in indoor residential AC circuits are typically lower than in industrial environments or outdoor AC power lines.

The primary protection is typically achieved with transient protectors like Zener diodes and metal-oxide varistors (MOV), which limit the voltage to a fixed level, by diverting the rest of the energy. Zener diodes are typically faster than MOVs; however, MOVs are generally available with higher Joule rating, making them more robust to power line disturbances. For primary power protection or outdoor systems, a gas discharge tube can be added between line and earth.

The voltage rating of the protective device should be selected sufficiently high to avoid clamping during low voltage swells. A margin of minimum 25-30% above the nominal line voltage is recommended.

Care should be taken that the transient protectors do not add a low impedance load at the communication frequency, which could attenuate the transmitted or received signals. The protective device capacitance must be particularly considered.

### 9.4.2 Coupling Methods

PLC coupling circuits can be classified in two categories: capacitive couplers and inductive couplers.

#### 9.4.2.1 Capacitive Coupling

The capacitive coupling is the method used in most applications, since it requires direct parallel connection with the communication channel. The main coupling element is a capacitor that blocks the line voltage, while passing the high-frequency communication signals. The capacitor has to be suited for the

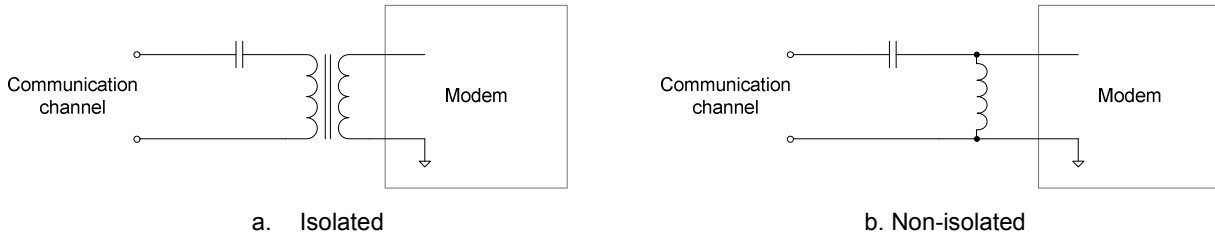


Figure 9-9 Capacitive coupling

line voltage. In addition to the coupling capacitor, an inductor or transformer is typically used to create a high-pass filter. The values of these components are chosen so that their impedance at the communication frequency is low, while the impedance at the line voltage frequency is high.

Isolated or non-isolated capacitive couplers can be designed (Figure 9-9), depending on the safety requirements for the intended product. The isolation is typically provided by a low-voltage transformer with appropriate characteristics at the communication frequency, as described in 9.4.1.2. While two-winding 1:1 transformers are more commonly available, three-winding transformers with different turns ratio can be used to amplify the communication signal in reception and/or in transmission. Table 9-4 provides a few examples of recommended coupling transformers.

Non-isolated couplers can be preferred in price-sensitive devices when there is no potential electrical shock hazard for the user.

**9.4.2.1.1 Line-to-Neutral and Line-to-Earth Coupling**

In mains power systems the capacitive coupling is traditionally used with live and neutral wires, available at every outlet. However, the electrical devices and appliances connected on the line between the same wires create low impedance and add noise in the communication frequency band. One way to avoid these severe conditions is to use the earth wire as return path for the signal.

While line-to-earth coupling typically provides better communication performance, the use of the ground (earth) wire can be prohibited by local regulations. Also, a practical limitation of line-to-earth coupling comes from the presence of ground fault interrupters, which can limit the maximum ground current to about 4mA. Generally, line-to-neutral coupling is recommended for in-home devices, while line-to-earth can be considered for commercial and industrial applications.

Part number	Manufacturer	Turns Ratio	Min Primary Inductance	Max DC Resistance	Max Isolation Voltage
MTN13453	Ariane Controls	1:1	1.2mH	160mΩ	500V
MTN13420	Ariane Controls	1:3	1.2mH	160mΩ	500V
MTN13417	Ariane Controls	1:3:0.6	1.2mH	160mΩ	500V
T60403-K5024-X044	Vacuumschmelze	1:1	1.4mH	200mΩ	6000V
T60403-K5024-X078	Vacuumschmelze	1:1	2.5mH	200mΩ	3000V
76601/2C	Murata	1:1	0.5mH	800mΩ	500V
78601/2C, 78601/2MC	Murata	1:1	0.5mH	340mΩ	1000V

Table 9-4 Examples of coupling transformers

### 9.4.2.1.2 Three-phase Coupling Circuits

In three-phase power systems, when transmitters and receivers are connected on different phases, the PLC signal should be coupled on the three lines to avoid signal loss between phases. The return path can be either neutral or earth, whichever is appropriate for the application.

Figure 9-10 shows the schematic of a typical three-phase coupler with one isolation transformer and three coupling capacitors. MOV protection devices and capacitor discharge resistors are also included. The three-phase coupler can be associated to a central transceiver (e.g., in master-slave topology) or can be designed as a stand-alone device, usually installed at the distribution panel.

Since a three-phase transmitter must drive the global parallel impedance of all phases, using a higher current Tx amplifier is recommended for such devices. In highly loaded three-phase power systems, three independent line drivers and coupling circuits can be used.

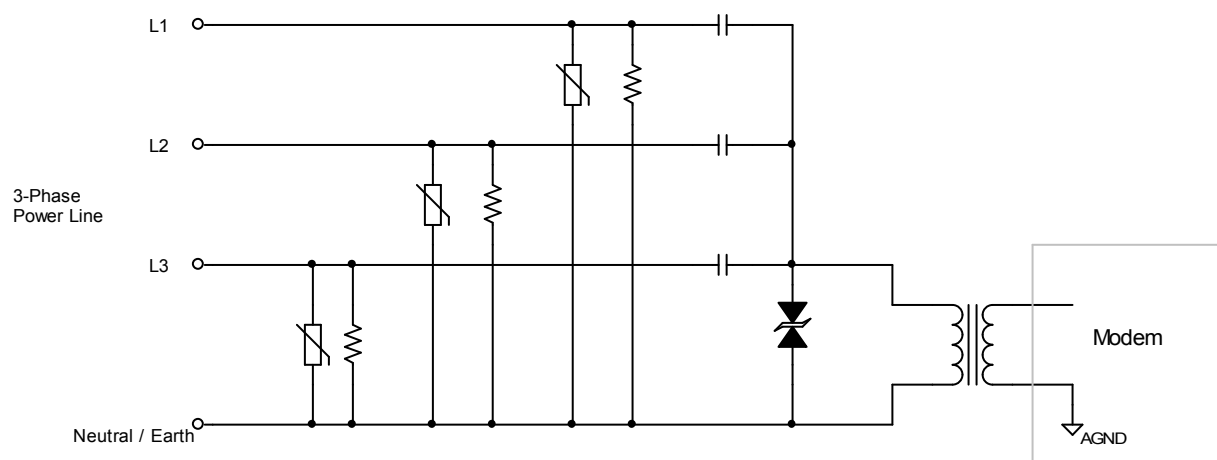
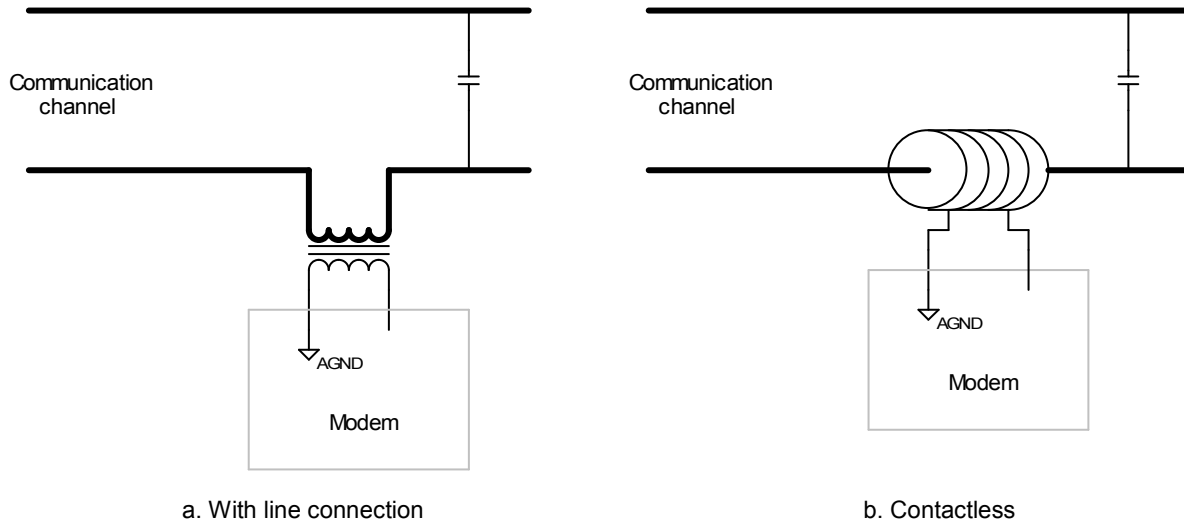


Figure 9-10 Three-phase isolated capacitive coupling circuit

### 9.4.2.2 Inductive Coupling

The inductive couplers are connected in series on the communication channel and inject a PLC current signal on the line. This is achieved through a specialized current transformer using appropriate high-frequency ferrites. The transformer also provides galvanic isolation.

Inductive couplers can be with or without connection to the communication cable (Figure 9-11). The couplers that require physical connection to the line have a low-current primary winding on the modem side and a high-current secondary winding connected in series on the line. This winding must be able to support the maximum line current. In contactless couplers the communication cable passes through the magnetic core and acts as a half-turn secondary winding. While contactless couplers don't require high-current winding and are easier to install, they provide lower coupling efficiency. In both inductive coupling variants, the coupling efficiency can be improved by adding a capacitor in parallel on the line to reduce the impedance at the coupling point and thus limit the signal return path.



**Figure 9-11 Inductive coupling**

As inductive couplers are connected in series on the line, they can be effectively used to avoid the signal attenuation caused by low parallel impedance. However, since they need to be inserted on the cable, the inductive couplers are mainly useful in applications that require permanent installation (industrial control systems, for example). Also, contactless inductive coupling is well suited for medium and high voltage power lines, where the size and cost of coupling capacitors become prohibitive.

## 9.5 AFE Reference Designs

A few examples of complete analog front-end schematics, intended to address the most typical applications, are provided in Appendix B. These schematics regroup filter, line driver and coupling circuits designs described in this section. The required component specifications with example part numbers and suppliers are provided.

The reference design of Appendix B1, based on 4<sup>th</sup>-order active filters in transmission and reception, is particularly useful for evaluation and prototyping. The Ariane Active Filter Designer software allows easy adjustment for testing various communication frequencies and data rates.

The second design, based on passive filters and discrete line driver, is a more cost-effective option intended for large scale installations.

While the first two circuits follow the requirements of FCC Part 15, the design of Appendix B3 uses more selective 8<sup>th</sup>-order active filter in transmission and is recommended for applications where the compliance with CENELEC requirements for conducted emissions is mandatory.

Finally, the schematic of Appendix B4, based on ceramic filters and class B push-pull line driver, is typically used for applications where compliance with conducted emissions regulations is not mandatory (e.g., communication on DC line or un-powered line).

## 10 Power Supplies for PLM-1 Transceivers

The power supply characteristics are very important for the overall performance of the PLC transceiver. When selecting or designing a power supply circuit, it is important to make sure that it does not harm the communication performance.

### 10.1 Power Supply Characteristics

Below are described the main parameters to be considered when selecting or designing a power supply for PLC transceivers.

#### 10.1.1 Output Power

The power supply must be capable of providing the DC current required for the transceiver operation. The supply voltage and current depend on the analog front-end design (i.e., Tx and Rx filters, line driver), as well as additional components like microcontroller, application interfaces (e.g., RS232, RS485, USB), LEDs, etc.

The average supply current in idle mode and during reception is typically low, for example from about 25mA for a basic transceiver up to 100mA for a complete evaluation board with several interfaces.

The maximum power consumption is in transmitting mode and depends on the impedance of the communication line. For transmitting the maximum signal possible in low impedance conditions, the transceiver power supply should be able to provide high peak currents for short periods during transmission. The transmission duration depends on data rate and message length. For example, when communicating at 4500bps, the transmission time typically ranges between 90ms for a 10-byte message and 350ms for a 63-byte message.

As a general rule, in order to ensure good communication performance, a power supply of 6 Watt or more is recommended with PLM-1 transceivers.

#### 10.1.2 Input Impedance

More often than not the supply input terminals are connected to the communication medium, i.e. AC or DC line. If the power supply input impedance at the communication frequency is too low, it can considerably attenuate both transmitted and received signals.

This loading effect can be avoided by adding an appropriate inductor in series between the power supply input and the communication channel, as shown in Figure 10-1.

The value of this inductor should provide a power supply input impedance sufficiently high to avoid extra

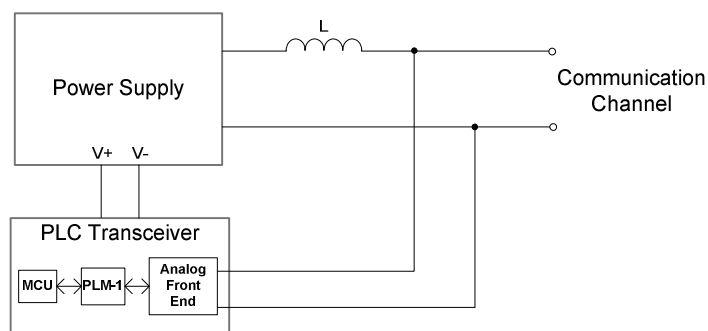


Figure 10-1 Increasing the input impedance of power supply by adding a series inductor

signal attenuation, i.e. usually 100Ω or more. Also, in order to avoid saturation, the series inductor must be rated for the peak current drawn by the power supply.

### 10.1.3 Noise

A power supply has the potential to degrade the transceiver performance by adding noise in the communication frequency range. Switching-mode power supplies (SMPS) and regulators are particularly challenging and their switching frequency should be carefully considered.

Noise can be generated by a power supply at the AC input terminals, as well as at the DC output. SMPS may couple significant noise at the switching frequency or its harmonics back onto the mains power line. Such noise generated close to a receiving PLC device can disturb the reception of low communication signals.

Also, a SMPS or a DC/DC switching regulator with improperly filtered output can produce noise and ripple on the DC supply voltages. The most critical for the PLC performance is the noise on the DC voltages of the Rx circuit (e.g., Rx filter, voltage comparator).

Adequate filtering and careful selection of the switching supply operating frequency are required to avoid the effect of the noise on the communication performance. The switching frequency and its harmonics should be outside the communication band, ideally greater than the communication frequency.

## 10.2 Power Supply Options

### 10.2.1 Linear Power Supply

If the size and weight of a low frequency transformer are acceptable, a traditional linear power supply is a suitable choice for PLC transceivers. Linear power supplies do not affect the communication by signal attenuation or noise. Also, they provide safety isolation, are easy to design, have low part count and relatively low cost. Linear DC/DC regulators also have significantly lower output noise than switching devices.

However, linear power supplies and regulators have poor efficiency; at high load currents, they dissipate considerable energy, distributed as heat. This can be particularly problematic in applications where intensive transmissions are required. In order to optimize the heat dissipation, the voltage difference between supply's input and output should be reduced and linear regulators must be provided with appropriate heat sinks.

Figure 10-2 shows a typical example of linear power supply circuit, which provides  $V_{DD}$  and 3.3V DC.  $V_{DD}$  voltage is related to the AFE design, typically between 5V and 15V. The transformer and protective varistor have to be rated for the AC mains voltage. The transformer power should be 6VA or more and the secondary RMS voltage should be the same as  $V_{DD}$  DC voltage. The bridge rectifier (BR) must be rated for the peak current drawn by the transceiver circuit. Linear regulators (U1, U2) must be provided with adequate heat sink area.

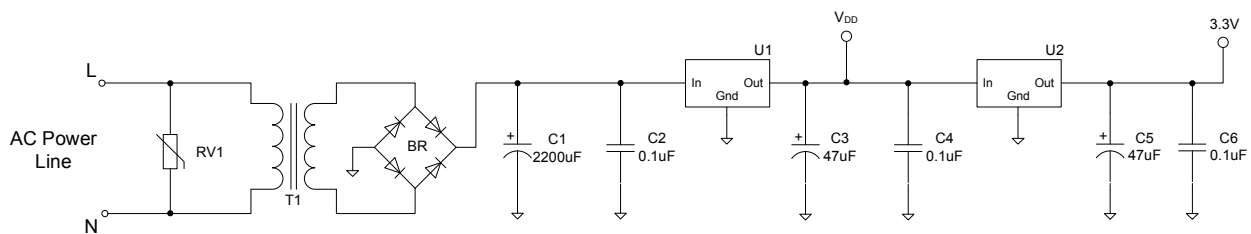


Figure 10-2 Linear power supply for PLC transceiver

## 10.2.2 Switching-mode Power Supply

Switching power supplies have superior efficiency and less heat dissipation than linear supplies, being more adequate for providing high load currents during long transmissions. Also, SMPS have generally smaller size, lower weight and universal input, being compatible with the mains voltage of most countries.

However, SMPS can be a significant source of noise and signal attenuation that may affect the communication performance. The attenuation is caused by the power supply capacitive EMC filter connected between line and neutral. In order to increase the input impedance and avoid the loading effect of the power supply, an appropriate inductor should be connected in series at the supply input, as shown in Figure 10-1. Generally, a minimum power supply input impedance of  $100\Omega$  is recommended to avoid additional signal attenuation.

The noise is related to the operating frequency of the switching device and can be coupled at both AC input and DC output terminals of the SMPS. When selecting or designing a SMPS for PLC transceivers, the switching frequency and its harmonics should avoid the communication frequencies.

The effect of AC line noise and signal attenuation of a SMPS can be avoided by adding an appropriate filter in series between the power supply and the mains. An example is shown in Figure 10-3. Both inductors must be rated for the peak AC current drawn by the power supply, while the capacitor needs to be rated for the line voltage.

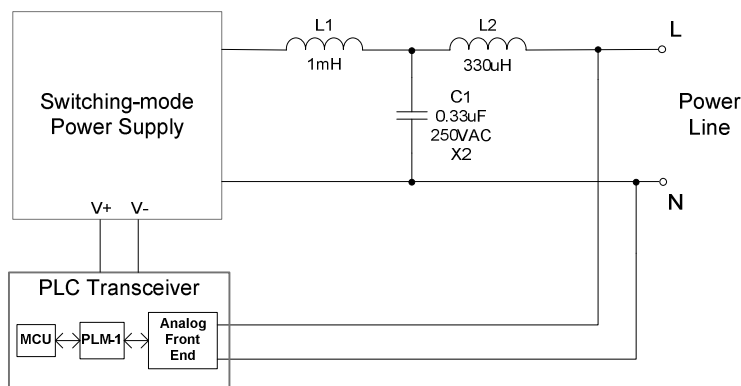


Figure 10-3 Additional filter at the input of SMPS to avoid noise and attenuation

## 10.2.3 Capacitive Power Supply

Considering the low current requirement in receiving mode, a transformerless capacitive power supply can be used with Rx-only devices. This type of supply provides a low-cost and low-size alternative to linear and switching power supplies, for applications requiring minimal current. However, the capacitive supply does not provide safety isolation between the power line and the low-voltage circuit.

Figure 10-4 shows an example of capacitive power supply able to provide an output current up to 50mA. The current capability of the supply is set by the input capacitor C1. The value of C1 is selected depending on the AC mains voltage. Table 10-1 gives a few values of C1 recommended for different AC voltages. C1, RV1 and R1 must be rated for the power line voltage. Also, C1 should be an X2 type capacitor.

Zener diode D1 acts as a shunt regulator and its nominal voltage sets the  $V_{DD}$  value. C2 capacitor is used as an energy storage reservoir. Since the available unused current flows through the shunt regulator, the Zener diode must be selected to handle the maximum peak and average power.

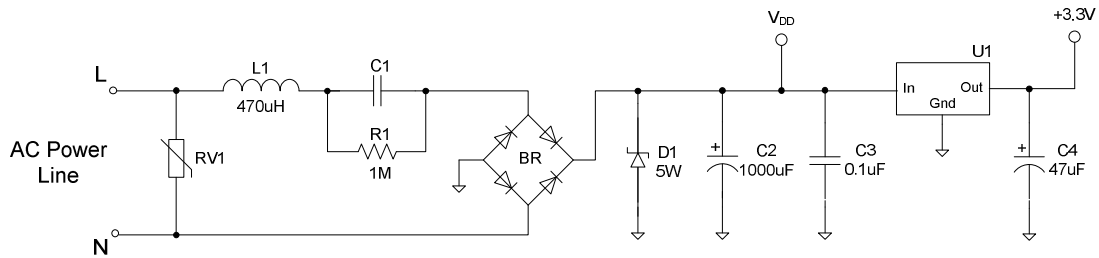


Figure 10-4 Low-current capacitive power supply for Rx only devices

AC mains voltage	C1
120V <sub>RMS</sub>	1.5uF
230V <sub>RMS</sub>	0.68uF
347V <sub>RMS</sub>	0.47uF

Table 10-1 C1 capacitor value for different AC mains voltages

L1 is used to increase the input impedance at communication frequency and avoid signal attenuation. The current rating of the inductor must be superior to the AC peak current drawn by the power supply.

### 10.2.4 Energy Storage Power Supply

For applications that require infrequent low-duty cycle transmissions, an energy storage circuit can be considered to reduce the size and cost of the power supply. Super-capacitors are available with high capacitance in relatively small package. By sizing the capacitor value to deliver the high peak current required during transmission, a low-current power supply can be used to provide the receive mode current plus an extra amount to recharge the storage capacitor between transmissions. The required reservoir capacitance mainly depends on the transmission duration and duty-cycle.

Special DC/DC switching regulators can be used to manage the charge of the super-capacitor. These devices can limit the input current to the maximum available from the power source. Also, they provide additional useful features like limiting the inrush current that can result during start-up, short-circuit and thermal overload protection, as well as an optional logic output that allows monitoring the voltage on the energy storage capacitor and then, if necessary, adjusting the time between transmissions so that the capacitor can recharge to the nominal voltage.

# 11 Transceiver Performance Verification

This section describes a simple testing methodology recommended to verify the performance of PLM-1-based transceivers. This procedure is not intended for validating the compliance with specific standards for powerline communication, but for determining in a known environment whether the transceiver operates properly prior to field deployment.

The following topics should be verified:

- Transmit performance
- Receive performance
- Transceiver influence on the communication channel

## 11.1 Test Setup

These tests are intended to be performed on an un-powered channel. This requires that the transceiver has separate connections to the communication channel and power supply, as shown in Figure 11-1.

The PLC channels of two transceivers under test are connected to a simple circuit composed of two series resistors ( $R_s$ ) and two parallel resistors ( $R_p$ ). The  $R_s$  resistors are intended to provide series attenuation of the transmit signal, while the  $R_p$  resistors provide parallel loading.

The wires between the transceivers and attenuation circuit should be kept short (15-20 cm). Power rating of 0.5Watt or more is recommended for the parallel  $R_p$  resistors.

An oscilloscope is required to measure the level of transmitted and received signals.

The results can be recorded using the table at the end of the section.

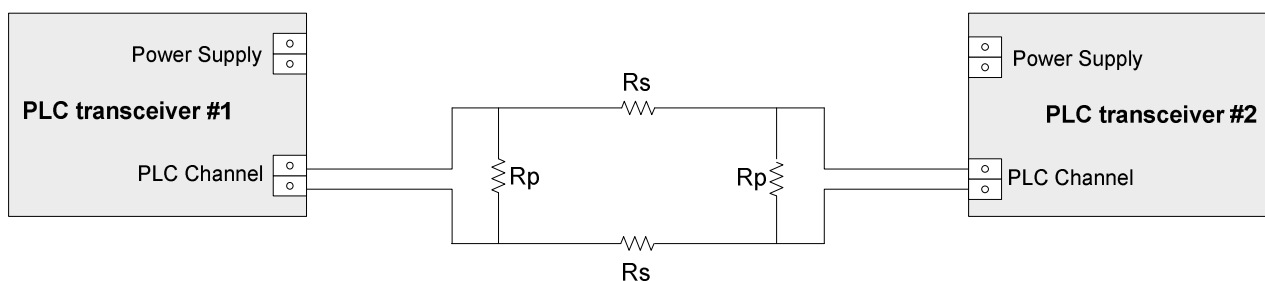


Figure 11-1 Test setup for transceiver performance verification

## 11.2 Transceiver Influence Verification

This test is intended to verify that the transceiver will not add excessive loading on the communication channel, which could increase the signal attenuation and affect the communication performance. Typically, a transceiver input impedance of minimum  $100\Omega$  at the communication frequency is recommended to avoid signal attenuation.

1. Set the attenuation circuit as follows: no  $R_p$ , no  $R_s$  (open circuit).
2. Start transmitting with transceiver #1 and measure the signal level ( $V_{p-p}$ ) at its output.
3. Connect the transceiver #2 by adding two  $R_s=0\Omega$  resistors into the circuit.
4. Measure again the level of the signal transmitted by transceiver #1. Compare to the previous measurement. The presence of transceiver #2 should not decrease considerably the signal transmitted by transceiver #1. Typically, the signal attenuation measured with this method should be less than 0.3dB.

The test can be repeated to verify the influence of transceiver #1 over the signal transmitted by transceiver #2.

## 11.3 Transmit Performance Verification

This test is used to verify the transmitter ability to drive low impedance loads.

5. Set the attenuation circuit as follows:  $R_p=50\Omega$ , no  $R_s$  (open circuit).
6. Measure the level of the signal transmitted by each transceiver across the  $R_p$  resistor connected at its output.
7. Set the attenuation circuit as follows:  $R_p=1\Omega$ , no  $R_s$  (open circuit).
8. Measure the level of the signal transmitted by each transceiver across the  $R_p$  resistor connected at its output.

The output signal can also be measured using different values for  $R_p$ , according to the typical line impedance of the intended application.

## 11.4 Receive Performance Verification

This test is intended to verify the transceiver receiving capability and measure the minimum level of accurately received signal when no additional noise is present on the line.

9. Set the attenuation circuit as follows:  $R_p=50\Omega$ ,  $R_s=0\Omega$ .
10. Start transmitting with transceiver #1 and monitor the reception at transceiver #2. The Packet Error Rate should be zero. Repeat the test by transmitting in opposite direction and monitor the reception at transceiver #1.
11. Change the attenuation circuit as follows:  $R_p=1\Omega$ ,  $R_s=10\Omega$ .
12. Start transmitting with transceiver #1 and monitor the reception at transceiver #2. The Packet Error Rate should be very close to zero. Repeat the test by transmitting in opposite direction and monitor the reception at transceiver #1.
13. Decrease  $R_p$  and/or increase  $R_s$  until the Packet Error Rate becomes close to 5% (using potentiometers can be helpful). Measure the level of the signal received by each transceiver across the  $R_p$  resistor connected at its input.

## 11.5 Summary of Results

The test results can be summarized using Table 11-1 below. It includes data for the evaluation of both transceivers under test.

Test no	Test description	Attenuation circuit settings	Measurement	Value	Comment
2	Transceiver #1 maximum output signal	No Rp, No Rs	$V_{out_{Tr1}}$ (Vp-p)		
4	Transceiver #2 influence	No Rp, Rs=0 $\Omega$	$V_{out_{Tr1}}$ (Vp-p)		
2	Transceiver #2 maximum output signal	No Rp, No Rs	$V_{out_{Tr2}}$ (Vp-p)		
4	Transceiver #1 influence	No Rp, Rs=0 $\Omega$	$V_{out_{Tr2}}$ (Vp-p)		
6	Transceiver #1 nominal output signal	Rp=50 $\Omega$ , Rs=open	$V_{out_{Tr1}}$ (Vp-p)		
6	Transceiver #2 nominal output signal	Rp=50 $\Omega$ , Rs=open	$V_{out_{Tr2}}$ (Vp-p)		
8	Transceiver #1 high-power output signal	Rp=1 $\Omega$ , Rs=open	$V_{out_{Tr1}}$ (Vp-p)		
8	Transceiver #2 high-power output signal	Rp=1 $\Omega$ , Rs=open	$V_{out_{Tr2}}$ (Vp-p)		
10	Transceiver #2 high signal reception	Rp=50 $\Omega$ , Rs=0 $\Omega$	PER (%)		
10	Transceiver #1 high signal reception	Rp=50 $\Omega$ , Rs=0 $\Omega$	PER (%)		
12	Transceiver #2 low signal reception	Rp=1 $\Omega$ , Rs=10 $\Omega$	PER (%)		
12	Transceiver #1 low signal reception	Rp=1 $\Omega$ , Rs=10 $\Omega$	PER (%)		
13	Transceiver #2 sensitivity (PER $\leq$ 5%)	Rp=var, Rs=var	$V_{in_{Tr2}}$ (Vp-p)		
13	Transceiver #1 sensitivity (PER $\leq$ 5%)	Rp=var, Rs=var	$V_{in_{Tr1}}$ (Vp-p)		

Table 11-1 Summary of test results

## 12 Appendices

### Appendix A Recommended PLM-1 Configurations

The following table provides several examples of PLM-1 configurations, recommended for different values of communication center frequency  $f_c$  and external clock frequency  $f_{osc}$ .

The subsequent columns include the PHY data rate ( $f_b$ ), the minimum -3dB bandwidth recommended for the external filters, and the four basic configuration parameters (CPB, CPT0, CPT1, and XDIV).

More PLM-1 configurations can be explored using the PLM-1 Configuration Tool, included in the ACES software.

Config No	$f_c$ (kHz)	$f_{osc}$ (MHz)	$f_b$ (bps)	Recommended filter BW <sub>-3dB</sub> (kHz)	CPB	CPT0	CPT1	XDIV
1	144	16	4535	4.5	36	7	6	98
2	144 <sup>1</sup>	14.31818	8117	8.1	21	5	4	84
3	144	10	5291	5.3	30	10	8	63
4	144	8	4535	4.5	36	7	6	49
5	262	20	3651	3.7	66	9	10	83
6	262	16	5013	5	56	14	12	57
7	262	10	2680	2.7	91	11	12	41
8	450	16	4010	4	105	12	13	38
9	450	10	5342	5.3	78	10	11	24
10	455	16	14337	14.3	36	7	6	31
11	455	13	18759	18.8	21	4	5	33

Table A-1 Recommended PLM-1 configurations and their basic communication parameters

---

<sup>1</sup> Configuration recommended for applications where the compliance with CENELEC EN 50065-1 is required.

## Appendix B Analog Front-End Reference Schematics

This appendix provides a few examples of complete analog front-end schematics and component information. The table below summarizes the characteristics of each design, with references to the recommended PLM-1 configurations of Appendix A.

The coupling circuits included in these designs are rated for operation at power line voltage up to 250V (AC or DC). However, the voltage rating of the coupling parts should be adapted to the actual communication medium.

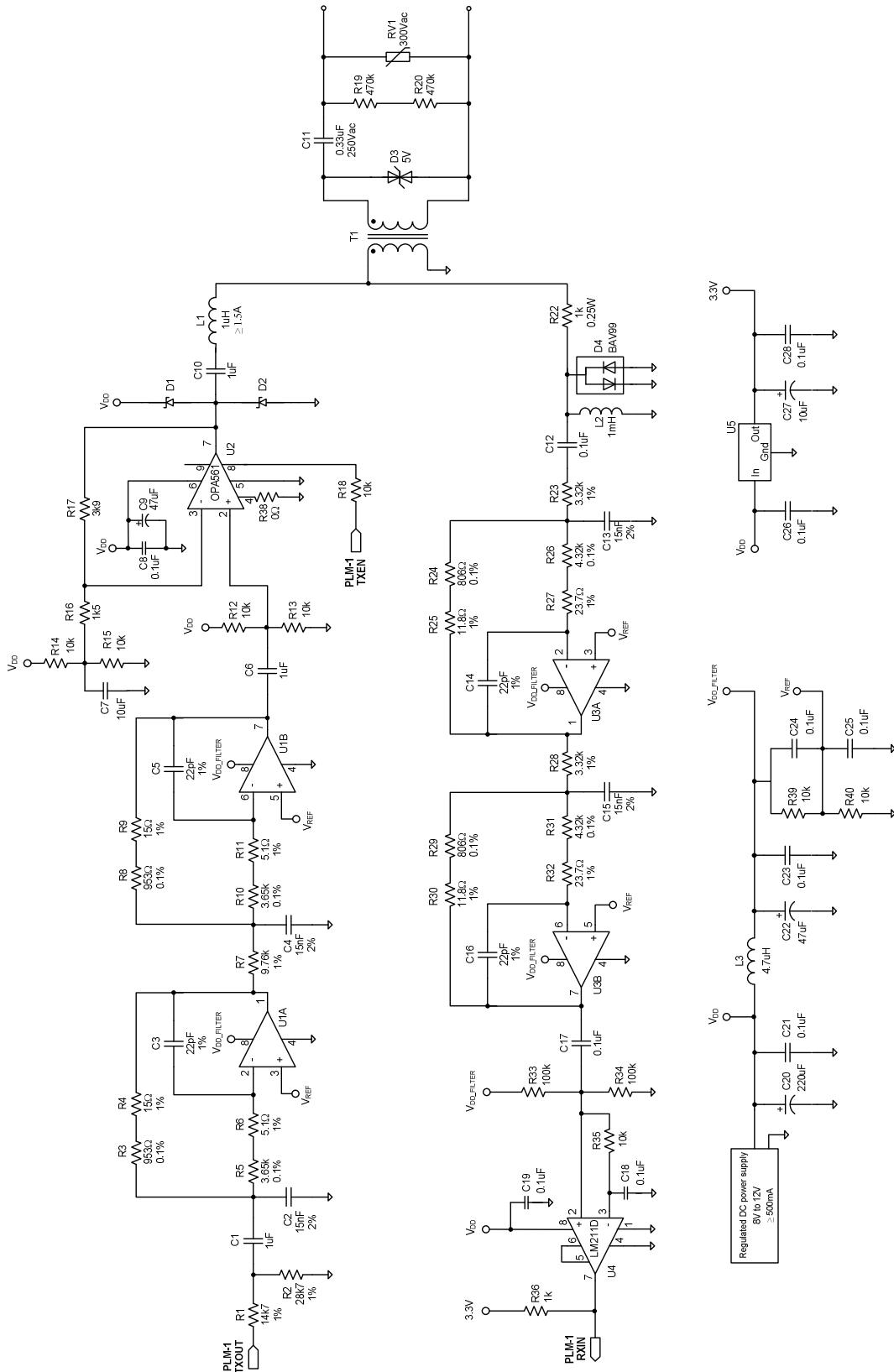
Example No.	Design type	Communication frequency	Max data rate	Regulation compliance	PLM-1 Configuration Examples <sup>1</sup>
B1	Active filters, OPA561 line driver, isolated capacitive coupling	144kHz	9kbps	FCC Part 15, ICES006	1 - 4
B2	Passive filters, discrete class AB line driver, isolated capacitive coupling	144kHz	9kbps	FCC Part 15, ICES006	1 - 4
B3	Active and passive filters, ACPL-0820 line driver, isolated capacitive coupling	144kHz	9kps	GENELEC EN 50065-1	2
B4	Ceramic filters, discrete class B line driver, isolated capacitive coupling	262kHz	5kbps	-	5 - 7
		455kHz	20kbps	-	10, 11

**Table B-1 Summary of AFE Examples**

---

<sup>1</sup> See the PLM-1 configuration table of Appendix A.

Example B-1 Active filters and OPA561 line driver (Fc=144kHz)



Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
C8, C12, C17, C18, C19, C21, C23, C24, C25, C26, C28	0.1uF	≥25V, Ceramic	GRM188R71E104KA01D (Murata)
C1, C6, C10	1uF	≥16V, Ceramic	ECJ-1VB1C105K (Panasonic)
C7	10uF	≥16V, Ceramic	EMK212BJ106KG-T (Taiyo Yuden)
C3, C5, C14, C16	22pF	≥16V, 1%, Ceramic NP0	06031A220FAT2A (AVX)
C9, C22	47uF	≥16V, Tantalum	B45197A3476K309 (Kemet)
C2, C4, C13, C15	0.015uF	≥16V, 2%, Ceramic NP0	C0603C153G3GACTU (Kemet)
C11	0.33uF	≥250V, X2 type <sup>1</sup>	ECQ-U2A334ML (Panasonic)
C20	220uF	≥16V, Tantalum	T491D227K016ZT (Kemet)
C27	10uF	≥10V, Tantalum	T491A106K010AT (Kemet)
D1, D2	Diode Schottky	≥30V, 3A	SSA33L-E3 (Vishay)
D3	TVS 5V	Bidirectional, 400Wpk	SMAJ5.0CA (Diodes, Littelfuse, Vishay)
D4	Diode dual	≥50V, 200mA, Switching	BAV99 (Diodes, NXP, Comchip Technology)
L1	1uH	≥1.5A, 10%	CPL2512T1R0M (TDK)
L2	1mH	≥30mA, 5%	ELJ-FB102JF (Panasonic)
L3	4.7uH	≥0.1A, 20%	CBC2016T4R7M (Taiyo Yuden)
R1	14.7kΩ	≥1/10W, 1%	RC0603FR-0714K7L (Yageo)
R2	28.7kΩ	≥1/10W, 1%	RC0603FR-0728K7L (Yageo)
R3, R8	953Ω	≥1/10W, 0.1%	TNPW0603953RBEEN (Vishay/Dale) RG1608P-9530-B (Susumu) RT0603BRD07953RL (Yageo)
R4, R9	15Ω	≥1/10W, 1%	RC0603FR-0715RL (Yageo)
R5, R10	3.65kΩ	≥1/10W, 0.1%	RG1608P-3651-B (Susumu Co)
R6, R11	5.1Ω	≥1/10W, 1%	RC0603FR-075R11L (Yageo)
R7	9.76kΩ	≥1/10W, 1%	RC0603FR-079K76L (Yageo)
R12, R13, R14, R15, R18, R35, R39, R40	10kΩ	≥1/10W, 1%	RC0603FR-0710KL (Yageo)
R16	1.5kΩ	≥1/10W, 1%	RC0603FR-071K5L (Yageo)
R17	3.9kΩ	≥1/10W, 1%	RC0603FR-073K9L (Yageo)
R19, R20	470kΩ	≥1/4W, ≥200V, 5% <sup>1</sup>	ERJ-8GEYJ474V (Panasonic)
R22	1kΩ	≥1/4W, 1%	ESR10EZPF1001 (Rohm)
R23, R28	3.32kΩ	≥1/10W, 1%	RC0603FR-073K32L (Yageo)
R24, R29	806Ω	≥1/10W, 0.1%	TNPW0603806RBEEN (Vishay/Dale) RG1608P-8060-B (Susumu) RT0603BRD07806RL (Yageo)
R25, R30	11.8Ω	≥1/10W, 1%	RC0603FR-0711R8L (Yageo)
R26, R31	4.32kΩ	≥1/10W, 0.1%	RG1608P-4321-B (Susumu Co)
R27, R32	23.7Ω	≥1/10W, 1%	RC0603FR-0723R7L (Yageo)
R33, R34	100kΩ	≥1/10W, 1%	RC0603FR-07100KL (Yageo)
R36	1kΩ	≥1/10W, 1%	RC0603FR-071KL (Yageo)
R38	0Ω	≥1/10W, 5%	RC0603JR-070RL (Yageo)
RV1	MOV	≥250VACrms, 0.25W <sup>1</sup>	ERZ-V07D471 (Panasonic)

## AC-PLM-1

---

Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
T1	Isolation Transformer 1:1	$\geq 500V_{rms}$ isolation, 0.5uH max leakage inductance	76601/2C, 76601/3C, 78601/2C, 78601/3C, 78601/2MC, 78601/3MC (Murata) MTN13453 (Ariane Controls)
U1, U3	Op Amp Dual	V-Feedback, High-Speed, High GBW, Low THD	TSH82IDT (ST Microelectronics) FHP3230IM8X (Fairchild Semiconductor) LMH6643MA (National Semiconductor) LT1813CS8 (Linear Technology)
U2	IC Line Driver <sup>2</sup>	High Output Current, High Output Voltage, High-Speed, High GBW, Low THD, Output Disable	OPA561PWP (Texas Instruments)
U4	Voltage Comparator	Differential, High speed, Low Input Offset	LM211D (Texas Instruments)
U5	3.3V Regulator	LDO, $\geq 100mA$	L4931ABDT33-TR (ST Microelectronics)

### Notes:

<sup>1</sup> The voltage rating of this part should be adapted to the line voltage.

<sup>2</sup> Adequate PCB heat sink area should be provided for the line driver IC. Refer to the OPA561 data sheet for guidelines on the layout design.



## AC-PLM-1

Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
C1, C13	100pF <sup>2</sup>	≥16V, Ceramic, 5%	C1608C0G1H101J (TDK)
C2, C14	22pF <sup>2</sup>	≥16V, Ceramic, 5%	C1608C0G1H220J (TDK)
C3, C15	15nF <sup>3</sup>	≥16V, Ceramic, 5%	C3216C0G1H153J (TDK)
C4, C16	11nF <sup>3</sup>	≥16V, Ceramic, 5%	GRM3195C1H113JA01D (Murata)
C5, C6, C8, C9, C10, C17, C18, C19, C20, C21, C23, C24, C26	0.1uF	≥16V, Ceramic, 10%	GRM188R71E104KA01D (Murata)
C7	6.8uF	≥16V, Tantalum, 10%	T491C685K025AT (Kemet)
C11	1uF	≥25V, Ceramic, 10%	GRM188R61E105KA12D (Murata)
C12	0.33uF	X2 type, ≥275V <sup>1</sup>	ECQ-U2A334ML (Panasonic)
C22	220uF	≥16V, Tantalum	T491D227K016ZT (Kemet)
C25	10uF	≥10V, Tantalum	T491A106K010AT (Kemet)
D1, D2, D4	Dual diode	≥50V, Fast recovery	BAV99 (Diodes, NXP, Comchip Technology)
D3	TVS 12V	Bidirectional, 400Wpk	SMAJ5.0CA (Diodes, Littlefuse, Vishay)
L1, L4	10mH	≥10mA, 5%, Q≥20@79.6kHz	NL565050T-103J-PF (TDK) B82442H1106K (Epcos)
L2, L5	47uH	≥10mA, 5%, Q≥50@2.5MHz	ELJ-FB470JF (Panasonic) NL453232T-470J-PF (TDK) CTMC1812F-470J (Central Technologies)
L3	1uH	≥1.5A, 20%	CPL2512T1R0M (TDK)
Q1	PNP	≥200mA, ≥25V	MMBT3906 (ON Semiconductor, Micro Commercial, Diodes, Fairchild, NXP)
Q2	NPN	≥200mA, ≥25V	MMBT3904 (ON Semiconductor, Micro Commercial, Diodes, Fairchild, NXP)
Q3	NPN	≥2A, ≥25V, High GBW <sup>4</sup>	MJD200 (ON Semiconductor)
Q4	PNP	≥2A, ≥25V, High GBW <sup>4</sup>	MJD210 (ON Semiconductor)
Q5	NPN	≥100mA, ≥25V	MMBT2222A (ON Semiconductor, Micro Commercial, Diodes, Fairchild, Infineon)
R1	255Ω	≥1/10W, 1%	RC0603FR-07255RL (Yageo)
R2, R3, R5, R6, R9, R26	10kΩ	≥1/10W, 1%	RC0603FR-0710KL (Yageo)
R4, R27	1kΩ	≥1/10W, 1%	RC0603FR-071KL (Yageo)
R7, R12, R13	300Ω	≥1/10W, 1%	RC0603FR-07300RL (Yageo)
R8	4.7kΩ	≥1/10W, 1%	RC0603FR-074K7L (Yageo)
R10	47kΩ	≥1/10W, 1%	RC0603FR-0747KL (Yageo)
R11, R23	3.9kΩ	≥1/10W, 1%	RC0603FR-073K9L (Yageo)
R14, R15	1Ω	≥1/2W, 10%	ERJ-14YJ1R0U (Panasonic)
R16, R17	470kΩ	≥1/4W, 5%, ≥200V <sup>1</sup>	ERJ-8GEYJ474V (Panasonic)
R18	255Ω	≥1/4W, 1%	RC1206FR-07255RL (Yageo)
R19	82kΩ	≥1/10W, 1%	RC0603FR-0782KL (Yageo)
R20	39kΩ	≥1/10W, 1%	RC0603FR-0739KL (Yageo)
R21	6.8kΩ	≥1/10W, 1%	RC0603FR-076K8L (Yageo)
R22	750Ω	≥1/10W, 1%	RC0603FR-07750RL (Yageo)
R24, R25	100kΩ	≥1/10W, 1%	RC0603FR-07100KL (Yageo)

Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
RV1	MOV	0.25W, $\geq 275\text{VACrms}$ <sup>1</sup>	ERZ-V07D471 (Panasonic)
T1	Isolation Transformer 1:1	$\geq 500\text{Vrms}$ isolation, 0.5uH max leakage inductance	76601/2C, 76601/3C, 78601/2C, 78601/3C, 78601/2MC, 78601/3MC (Murata) MTN13453 (Ariane Controls)
U1	Op Amp Driver	GBWP $\geq 5\text{MHz}$ , I <sub>out</sub> $\geq 50\text{mA}$ , Shutdown	TLC080 (Texas Instruments)
U2	Voltage Comparator	Differential, High speed, Low Input Offset	LM211D (Texas Instruments)
U3	3.3V Regulator	LDO, $\geq 100\text{mA}$	L4931ABDT33-TR (ST Microelectronics)

**Notes:**

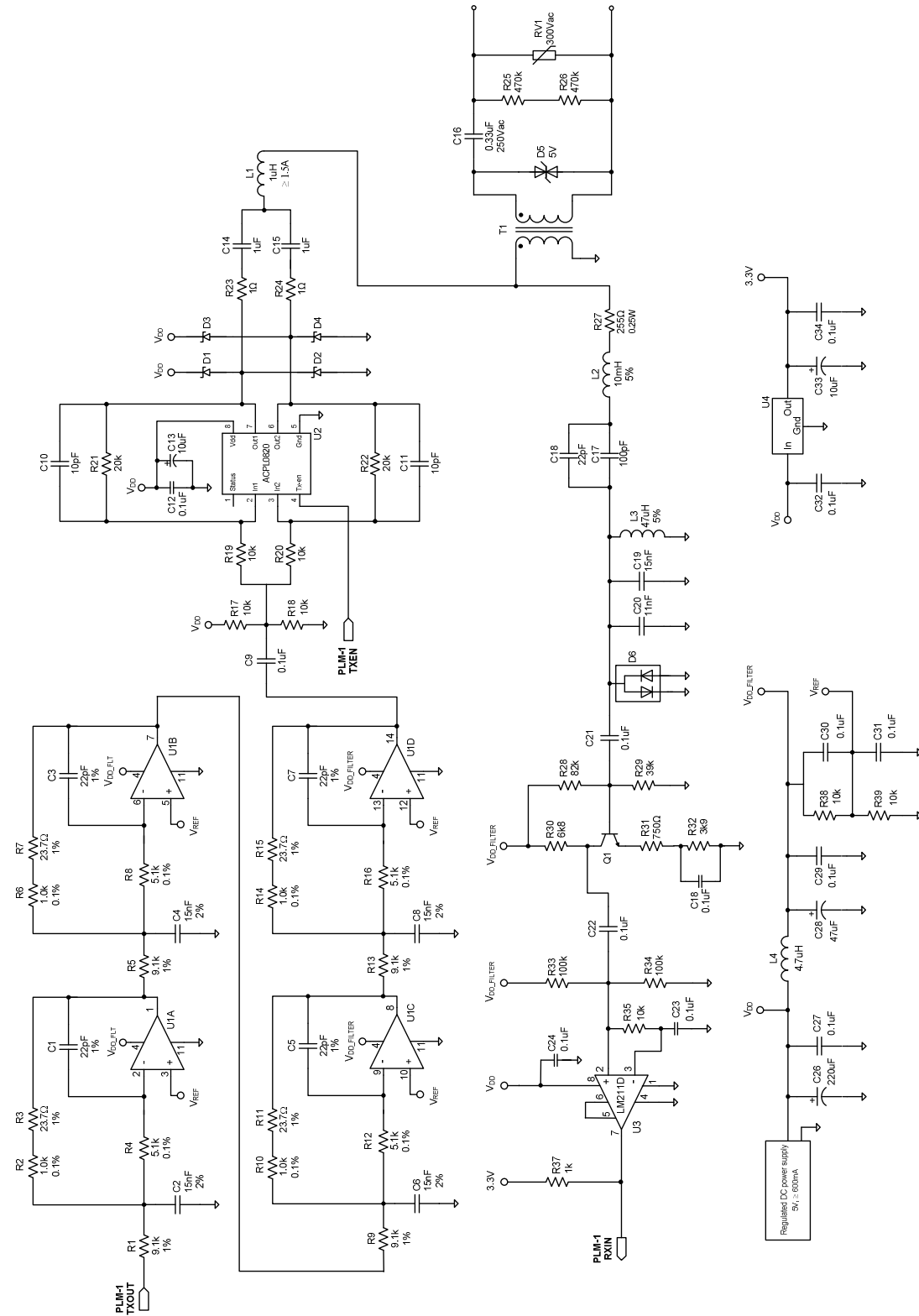
<sup>1</sup> The voltage rating of this part should be adapted to the line voltage.

<sup>2</sup> The values of these capacitors can be chosen so that their parallel combination is equal to 122pF.

<sup>3</sup> The values of these capacitors can be chosen so that their parallel combination is equal to 26nF.

<sup>4</sup> Adequate heat sink area should be provided for the push-pull output transistors.

Example B-3 Active filter for CENELEC compliance, ACPL-0820 line driver (Fc=144kHz)



Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
C1, C3, C5, C7	22pF	≥10V, 1%, Ceramic NP0	06031A220FAT2A (AVX)
C2, C4, C6, C8	0.015uF	≥10V, 2%, Ceramic NP0	C0603C153G3GACTU (Kemet)
C9, C12, C21, C22, C23, C24, C25, C27, C29, C30, C31, C32, C34	0.1uF	≥10V, Ceramic	GRM188R71E104KA01D (Murata)
C10, C11	10pF	≥10V, Ceramic	GRM1885C1H100JA01D (Murata)
C13, C33	10uF	≥10V, Tantalum	T491A106K010AT (Kemet)
C14, C15	1uF	≥10V, Ceramic	ECJ-1VB1C105K (Panasonic)
C16	0.33uF	≥250V, X2 type <sup>1</sup>	ECQ-U2A334ML (Panasonic)
C17	100pF <sup>2</sup>	≥10V, Ceramic, 5%	C1608C0G1H101J (TDK)
C18	22pF <sup>2</sup>	≥10V, Ceramic, 5%	C1608C0G1H220J (TDK)
C19	15nF <sup>3</sup>	≥10V, Ceramic, 5%	C3216C0G1H153J (TDK)
C20	11nF <sup>3</sup>	≥10V, Ceramic, 5%	GRM3195C1H113JA01D (Murata)
C26	220uF	≥10V, Tantalum	TAJD227K010RNJ (AVX)
C28	47uF	≥10V, Tantalum	TAJC476K010RNJ (AVX)
D1, D2, D3, D4	Diode Schottky	≥30V, 1A	SSA33L-E3 (Vishay)
D5	TVS 5V	Bidirectional, 400Wpk	SMAJ5.0CA (Diodes, Littlefuse, Vishay)
D6	Diode dual	≥50V, 200mA, Switching	BAV99 (Diodes, NXP, Comchip Technology)
L1	1uH	≥1.5A, 10%	CPL2512T1R0M (TDK)
L2	10mH	≥10mA, 5%, Q≥20@79.6kHz	NL565050T-103J-PF (TDK) B82442H1106K (Epcos)
L3	47uH	≥10mA, 5%, Q≥50@2.5MHz	ELJ-FB470JF (Panasonic) NL453232T-470J-PF (TDK) CTMC1812F-470J (Central Technologies)
L4	4.7uH	≥0.1A, 20%	CBC2016T4R7M (Taiyo Yuden)
R1, R5, R9, R13	9.1kΩ	≥1/10W, 1%	RC0603FR-079K1L (Yageo)
R2, R6, R10, R14	1.0kΩ	≥1/10W, 0.1%	RG1608P-102-B-T5 (Susumu)
R3, R7, R11, R15	23.7Ω	≥1/10W, 1%	RC0603FR-0723R7L (Yageo)
R4, R8, R12, R16	5.1kΩ	≥1/10W, 0.1%	RG1608P-512-B-T5 (Susumu Co)
R17, R18, R19, R20, R35, R38, R39	10kΩ	≥1/10W, 1%	RC0603FR-0710KL (Yageo)
R21, R22	20kΩ	≥1/10W, 1%	RC0603FR-0720KL (Yageo)
R23, R24	1Ω	≥1/2W, 10%	ERJ-14YJ1R0U (Panasonic)
R25, R26	470kΩ	≥1/4W, ≥200V, 5% <sup>1</sup>	ERJ-8GEYJ474V (Panasonic)
R27	255Ω	≥1/4W, 1%	RC1206FR-07255RL (Yageo)
R28	82kΩ	≥1/10W, 1%	RC0603FR-0782KL (Yageo)
R29	39kΩ	≥1/10W, 1%	RC0603FR-0739KL (Yageo)
R30	6.8kΩ	≥1/10W, 1%	RC0603FR-076K8L (Yageo)
R31	750Ω	≥1/10W, 1%	RC0603FR-07750RL (Yageo)
R32	3.9kΩ	≥1/10W, 1%	RC0603FR-073K9L (Yageo)
R33, R34	100kΩ	≥1/10W, 1%	RC0603FR-07100KL (Yageo)
R37	1kΩ	≥1/10W, 1%	RC0603FR-071KL (Yageo)
RV1	MOV	≥250VACrms, 0.25W <sup>1</sup>	ERZ-V07D471 (Panasonic)

## AC-PLM-1

---

Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
Q1	NPN	$\geq 100\text{mA}$ , $\geq 25\text{V}$	MMBT2222A (ON Semiconductor, Micro Commercial, Diodes, Fairchild, Infineon)
T1	Isolation Transformer 1:1	$\geq 500\text{Vrms}$ isolation, $0.5\mu\text{H}$ max leakage inductance	76601/2C, 76601/3C, 78601/2C, 78601/3C, 78601/2MC, 78601/3MC (Murata) MTN13453 (Ariane Controls)
U1	Op Amp Quad	V-Feedback, High-Speed, High GBW, Low THD	TSH84IPT (ST Microelectronics) FHP3430IM14X (Fairchild Semiconductor) LMH6644MA (National Semiconductor) LT1814 (Linear Technology)
U2	IC Line Driver <sup>4</sup>	High Output Current, High-Speed, High GBW, Low THD, Output Disable	ACPL-0820 (Avago)
U3	Voltage Comparator	Differential, High speed, Low Input Offset	LM211D (Texas Instruments)
U4	3.3V Regulator	LDO, $\geq 100\text{mA}$	L4931ABDT33-TR (ST Microelectronics)

### Notes:

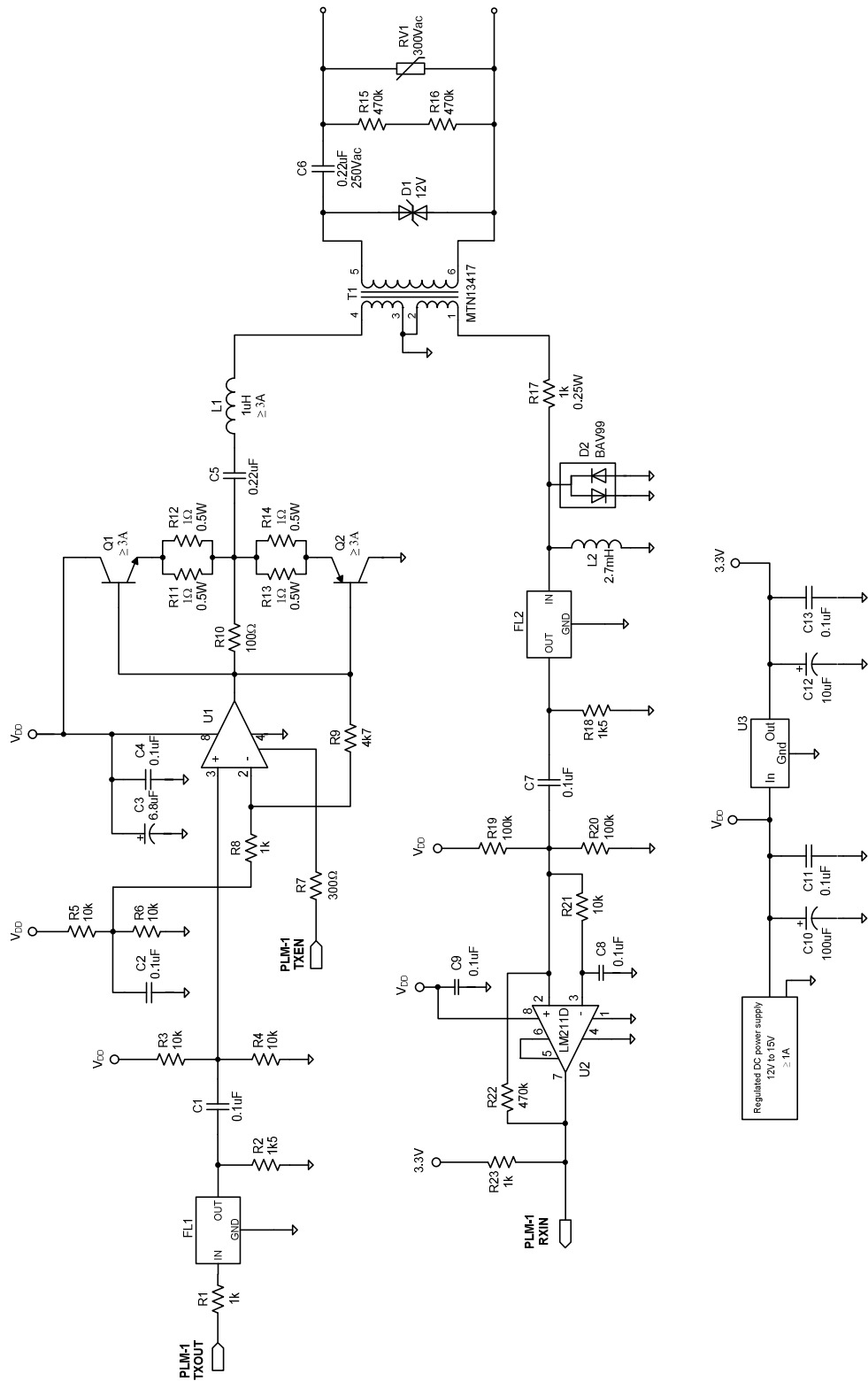
<sup>1</sup> The voltage rating of this part should be adapted to the line voltage.

<sup>2</sup> The values of these capacitors can be chosen so that their parallel combination is equal to  $122\text{pF}$ .

<sup>3</sup> The values of these capacitors can be chosen so that their parallel combination is equal to  $26\text{nF}$ .

<sup>4</sup> Adequate PCB heat sink area should be provided for the line driver IC.

Example B-4 Ceramic filters and discrete class B line driver ( $F_c=262\text{kHz}$  or  $F_c=455\text{kHz}$ )



## AC-PLM-1

Component	Value	Required Specifications	Example Part Numbers (Manufacturer)
C1, C2, C4, C7, C8, C9, C11, C13	0.1uF	≥25V, Ceramic	GRM188R71H104KA93D (Murata)
C3	6.8uF	≥25V, Tantalum	T491C685M035AT (Kemet)
C5	0.22uF	≥50V, Metalized film	B32529C1224K (Epcos)
C6	0.22uF	≥250V, X2 type <sup>1</sup>	ECQ-U2A224ML (Panasonic)
C10	100uF	≥25V, Tantalum	T491X107K025ZT (Kemet)
C12	10uF	≥10V, Tantalum	T491A106K010AT (Kemet)
D1	TVS 12V	Bidirectional, 400Wpk	SMAJ12CA (Diodes, Littelfuse, Bourns)
D2	Diode dual	≥50V, 200mA, Switching	BAV99 (Diodes, NXP, Comchip Technology)
FL1, FL2 <sup>2</sup>	Ceramic filter 262kHz	F <sub>c</sub> =262±1kHz, BW <sub>6dB</sub> ≥5kHz	FM262AL (Ariane Controls)
	Ceramic filter 455kHz	F <sub>c</sub> =455±1.5kHz, BW <sub>6dB</sub> ≥20kHz	CFUKF455KD1X-R0 (Murata)
L1	1uH	≥3A, 10%	NRS5020T1R0NMGJ (Taiyo Yuden)
L2	2.7mH	≥30mA, 5%	NL565050T-272J-PF (TDK)
Q1	NPN	≥3A, ≥25V, High GBW <sup>3</sup>	MJD200 (ON Semiconductor) MJD44H11 (Fairchild)
Q2	PNP	≥3A, ≥25V, High GBW <sup>3</sup>	MJD210 (ON Semiconductor) MJD45H11 (Fairchild)
R1, R8, R23	1kΩ	≥1/10W, 1%	RC0603FR-071KL (Yageo)
R2, R18	1.5kΩ	≥1/10W, 1%	RC0603FR-071K5L (Yageo)
R3, R4, R5, R6, R21	10kΩ	≥1/10W, 1%	RC0603FR-0710KL (Yageo)
R7	300Ω	≥1/10W, 1%	RC0603FR-07300RL (Yageo)
R9	4.7kΩ	≥1/10W, 1%	RC0603FR-074K7L (Yageo)
R10	100Ω	≥1/10W, 1%	RC0603FR-07100RL (Yageo)
R11, R12, R13, R14	1Ω	≥1/2W, 10%	ERJ-14YJ1R0U (Panasonic)
R15, R16	470kΩ	≥1/4W, ≥200V, 5% <sup>1</sup>	ERJ-8GEYJ474V (Panasonic)
R17	1kΩ	≥1/4W, 1%	ESR10EZPF1001 (Rohm)
R19, R20	100kΩ	≥1/10W, 1%	RC0603FR-07100KL (Yageo)
RV1	MOV	≥250VACrms, 0.25W <sup>1</sup>	ERZ-V07D471 (Panasonic)
T1	Isolation Transformer	≥500Vrms isolation, 3 windings	MTN13417 (Ariane Controls)
U1	Op Amp Driver	GBWP≥5MHz, I <sub>out</sub> ≥50mA, Shutdown	TLC080 (Texas Instruments)
U2	Voltage Comparator	Differential, High speed, Low Input Offset	LM211D (Texas Instruments)
U3	3.3V Regulator	LDO, ≥100mA	L4931ABDT33-TR (ST Microelectronics)

### Notes:

<sup>1</sup> The voltage rating of this part should be adapted to the line voltage.

<sup>2</sup> For both FL1 and FL2, select 262kHz or 455kHz ceramic filters.

<sup>3</sup> Adequate heat sink area should be provided for the push-pull output transistors.

## References

- [1] *FCC, Title 47, Part 15, Subpart B – Unintentional Radiators*, The Federal Communications Commission, December 8, 2003
- [2] ICES-006, AC Wire Carrier Current Devices (Unintentional Radiators), Industry Canada, Issue 1, August 25, 2001
- [3] *CENELEC EN50065-1:2001, Signalling on low-voltage electrical installations in the frequency range 3kHz to 148.5kHz*, European Committee for Electrotechnical Standardization, 2001
- [4] *Ron Mancini, Op Amps for Everyone – Reference Design*, Texas Instruments, August 2002

## **INFORMATION**

For further information on Ariane Controls technology and products,  
please visit our web site:

[www.arianecontrols.com](http://www.arianecontrols.com)

## **CONTACT**

ARIANE CONTROLS

2145 Chemin Sainte-Foy, suite 22  
Quebec, QC, G1V 1S1  
Canada

Tel: +1.418.874.1919  
Fax: +1.418.872.4348

Sales: [sales@arianecontrols.com](mailto:sales@arianecontrols.com)  
Technical support: [support@arianecontrols.com](mailto:support@arianecontrols.com)